
CRITICAL RECORDING.
RELIABLE SOLUTIONS.
High Speed, Real-Time
Recording Solutions for
Rugged UAV applications.
FREE Evaluation!
SystemFlow
Simulator
TALON
R7X EXTREME
RECORDER
PENTEK

Military EMBEDDED SYSTEMS

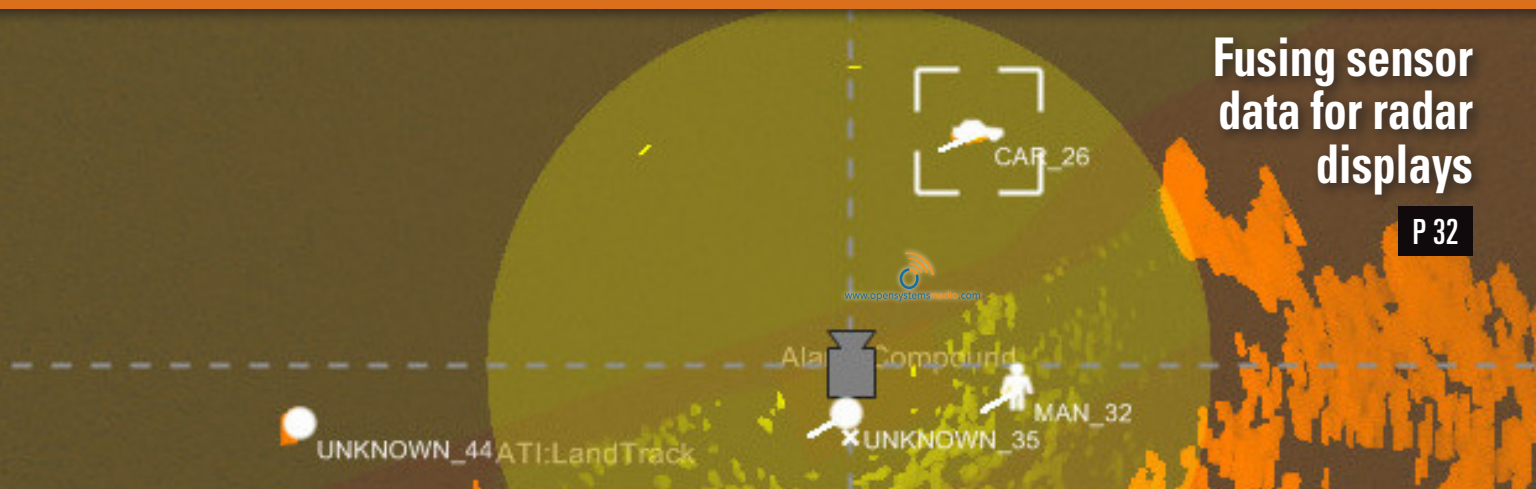
January 2014
Volume 10 | Number 1
MIL-EMBEDDED.COM

RADAR ISSUE

EMBEDDED SIGNAL PROCESSING ENABLES ADVANCED RADARS WITH LOW LATENCY

P 20

ISR as a Service: Providing users with affordable surveillance and reconnaissance – By Robert Smith, Lockheed Martin



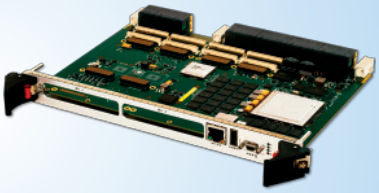
Fusing sensor data for radar displays

P 32

Module and System-Level Solutions from X-ES

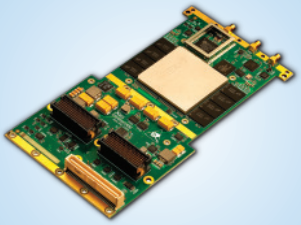
Intel® and Freescale™ Single Board Computers

XPedite7570
4th Gen Intel® Core™ i7-based 3U VPX SBC with XMC/PMC



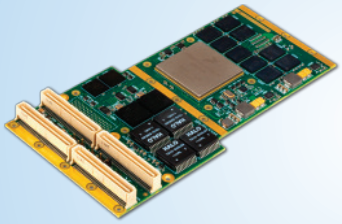
XCalibur1840
Freescale QorIQ T4240-based 6U VPX SBC with dual XMC/PMC

High-Performance FPGA and I/O Modules



XPedite2400
Xilinx Virtex-7 FPGA-based XMC with high-throughput DAC

Secure Ethernet Switches and IP Routers



XPedite5205
Secure Gigabit Ethernet router XMC utilizing **Cisco™ IOS®**

XChange3018
3U VPX 10 Gigabit Ethernet managed switch and router

High-Capacity Power Supplies

XPm2220
3U VPX 300W power supply with EMI filtering for MIL-STD-704 & 1275

Rugged, SWaP-Optimized, COTS-Based Systems

XPand4200
Sub-½ ATR, 6x 3U VPX slot system with removable SSDs

XPand6200
SFF 2x 3U VPX system with removable SSD and integrated power supply

XPand6000
SFF Intel® Core™ i7 or Freescale QorIQ-based system with XMC/PMC

X-ES
Extreme Engineering Solutions
608.833.1155 www.xes-inc.com

Designed, manufactured, and supported in the USA

Annapolis Micro Systems

The FPGA Systems Performance Leader

WILDSTAR OpenVPX Ecosystem

FPGA Processing Boards
1 to 3
Altera Stratix V or
Xilinx Virtex 6 or 7
FPGAs per Slot

Input/Output Modules Include:
Quad 130 MSps thru Quad 550 MSps A/D
1.5 GSps thru 5.0 GSps A/D
Quad 600 MSps D/A
Dual 1.5 GSps thru 4.0 GSps D/A

1 to 40 Gbit Ethernet
SDR to FDR Infiniband

Open VPX Storage
Up to 8 TBytes Per Slot
4 - 8 GBytes Per Second

GEOINT, Ground Stations, SDR, Radar, Sigint, COMINT, ELINT, DSP, Network Analysis, Encryption, Image Processing, Pattern Matching, Oil & Gas Exploration, Financial and Genomic Algorithms,

Open VPX Switch
1 to 40 Gbit Ethernet
SDR to FDR Infiniband

Chassis
4, 6 or 12 Slot
Up to 14G

Annapolis Micro Systems

High Performance Signal and Data Processing in Scalable COTS FPGA Computing Fabric

190 Admiral Cochrane Drive, Suite 130, Annapolis, Maryland USA 21401
wfinfo@annapmicro.com USA (410) 841-2514 www.annapmicro.com

www.mil-embedded.com

Military EMBEDDED SYSTEMS

ON THE COVER:

Top photo: Raytheon's Patriot Air and Missile Defense System's radar for Taiwan and Saudi Arabia upgraded from a VME technology to a OpenVPX-based system from Mercury Systems. Photo courtesy of Raytheon

Bottom photo: This photo shows track data and radar video from two sensors. Photo courtesy of Cambridge Pixel.

January 2014 | Volume 10 | Number 1

COLUMNS

DEPARTMENTS

E-CASTS

http://ecast.opensystemsmedia.com

Innovation in radar and electronic warfare systems through signal processing

Presented by GE Intelligent Platforms, Pentek, Mercury Systems, Thermacore
http://ecast.opensystemsmedia.com/445

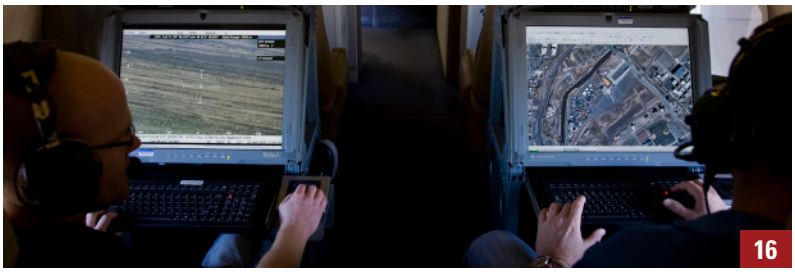
Maximizing system performance in time and space partitioned DO-178-certifiable safety-critical systems

Speaker: Tim King, DDC-I
http://ecast.opensystemsmedia.com/447

WEB RESOURCES

Subscribe to the magazine or E-letter
Live industry news | Submit new products
http://submit.opensystemsmedia.com

White papers:
Read: http://whitepapers.opensystemsmedia.com
Submit: http://submit.opensystemsmedia.com



Published by: OpenSystems media

ISSN: Print 1557-3222

@military_cots

www.linkedin.com/groups/Military-Embedded-Systems-1864255

Primary Radar is Our Passion

Simulation, Display, Tracking, Recording, Open Standards Network Distribution

Whether you're radar manufacturer or systems integrator, Cambridge Pixel's hardware-agnostic open-systems approach puts you in control offering freedom, flexibility, reduced through life costs and ease of technology refresh.

Simulation with ASTERIX tracks and video

Our newly announced SPx Simulator with optional HPx-300 Radar Output hardware supports the development of complex multi-radar, multi-target scenarios to generate representative primary radar, AIS, NMEA, navigation, ASTERIX CAT-48, CAT-34 and CAT-240 messages.

Radar Toolkit

The Cambridge Pixel family of radar components covers scan conversion, network streaming, target tracking and recording. We offer modular toolkits for developers and we provide cost-effective ready-to-run applications for PC-based radar display and tracking under Windows and Linux.

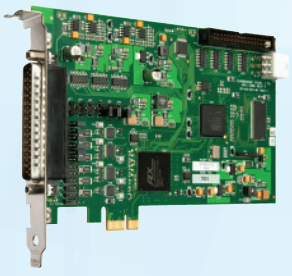
The Cambridge Pixel Approach

Our approach is to provide flexible, easy-to-use modules of software. We can supply complete turn-key solutions or individual software modules for inclusion in a customer's existing application. And it is all backed by Cambridge Pixel's do-what-it-takes technical support to help you when you need it.

New HPx-300 Radar Output

The new HPx-300 Radar Output Card generates radar video signals for system testing, simulation, training and video streaming

- Highly configurable output signals
- Output timing synchronised to input data
- Video (x2), Trigger, ACP/ARP, SHM, parallel azimuth
- Configurable scan rates, PRFs
- Compact half length PCIe card
- Available with SPx Simulator and Development software



Cambridge Pixel Ltd
New Cambridge House
Litlington Royston
Herts SG8 0SS UK
T: +44 1763 852749
enquiries@cambridgepixel.com
www.cambridgepixel.com

Tech Source
442 Northlake Blvd,
Altamonte Springs,
FL 32701, USA
T: 407-262-7100
embeddedgraphics@techsource.com
www.techsource.com

CAMBRIDGE PIXEL
SENSOR PROCESSING & DISPLAY SOLUTIONS

Learn more about our products here

ADVERTISER INFORMATION

Page	Advertiser/Ad Title
14	**ACCES I/O Products, Inc.** – USB embedded I/O solutions – Rugged, industrial strength USB
42	**AIM-USA** – What's in the box?
3	**Annapolis Micro Systems, Inc.** – WILDSTAR OpenVPX ecosystem
45	**Annapolis Micro Systems, Inc.** – COTS WILD OpenVPX ecosystem
45	**Annapolis Micro Systems, Inc.** – WILDSTAR FPGA COTS processing boards
45	**Annapolis Micro Systems, Inc.** – COTS WILD data storage solution
23	**Avionics Interface Technologies** – Test instrumentation
5	**Cambridge Pixel** – Primary radar is our passion
21	**Data Device Corporation** – Enabling more...
43	**Diamond Systems Corporation** – Rugged Gigabit Ethernet switches
30	**Elma Electronic** – SigPro1: Signal acquisition, FPGA-based record/ playback system
46	**Embedded World** – Summit for innovations
39	**Evans Capacitor Company** – Evanscaps everywhere
19	**Excalibur Systems, Inc.** – Dragon – it's not a myth
47	**GE Intelligent Platforms, Inc.** – High-performance RADAR with out-of-box readiness
37	**Interface Concept** – SBCs premium Intel and Freescale processors
44	**Kimdu Corporation** – Protocol converters
27	**LCR Embedded Systems** – Rugged systems engineered for your application
35	**Mercury Systems** – Innovation that detects
48	**Pentek, Inc.** – Got tough software radio design challenges?
34	**Phoenix International** – Rugged deployable RAID data storage
31	**Proto Labs** – Others say they're FAST ... but do they have the scale to deliver?
44	**Rakon** – Rakon's digital pulse compression sub-systems
15	**SynQor** – Uninterruptible power supply
44	**Thermacore International, Inc.** – Thermacore delivers thermal performance advantages in the world's hottest spots
44	**Wind River Aerospace & Defense Division** – Safety-critical market leader
2	**X-ES** – Module and system-level solutions from X-ES
44	**X-ES – XPedite2470** – Virtex-7 FPGA-based 3U OpenVPX module
44	**X-ES – XPand6208** – High-performance small form factor system

Military EMBEDDED SYSTEMS

OpenSystems media®

Radar market promising for embedded computing designers

By John McHale, Editorial Director

Welcome to our 2014 Radar Issue. Why have an issue focused on radar? Simple: the radar market, along with Electronic Warfare (EW), shows the most promise for embedded-computing system designs.

As Brad Curran, an analyst with Frost & Sullivan says, "Radar is hot. In 2011 there were 79 radar contracts totaling $3.27 billion with Raytheon as the leading producer. In 2012 the total contracts increased to 88, worth $4.26 billion, with Raytheon again as the leader. In 2013 there were 79 radar contracts totaling $4.03 billion, with Raytheon leading again with 24 of the contracts for $2.09 billion."

Raytheon's reign at the top of the radar world looks to continue for a while, especially with their win of the U.S. Navy's Air and Missile Defense Radar (AMDR) contract – a next-generation defensive system for Arleigh Burke-class destroyers. The new radar will enhance ships' ability to detect ballistic missiles, as well as air and surface targets, according to Raytheon. The AMDR will be scalable, working with any ship or mission. It will make use of digital beamforming to provide wide-area surveillance while gaining high precision with multiple, simultaneous radar beams. It will also have a radar resource scheduler to allow it to perform multiple missions simultaneously without extending the demand on the ship's prime power system. It is based on other Raytheon active phased-array radars, which make use of sometimes thousands of individual transmitters on each radar face to steer signals electronically, according to a Raytheon release.

Maritime radar is also a growth market, Curran says. "For 2013 there were 41 contracts for $1.59 billion, with Raytheon leading. This trend will continue as ballistic-missile defense upgrades for Aegis ships and anti-ship missile defenses are a priority, along with airborne maritime surveillance as the P-8, Triton Dome, and other Unmanned Aerial Vehicles (UAVs) are deployed." For more on maritime radar and Raytheon, see Senior Editor Sally Cole's Special Report on page 12.

The market has a mix of new radar designs and upgrades of signal-processing systems. "Radar retrofits typically involve a switch from VME to VPX systems in a shelf upgrade," says Bill Pilaud, Continuum HPEC Manager for Curtiss-Wright Controls Defense Solutions in Ashburn, VA. "VPX provides such a large improvement in threat-detection capability that it is hard to resist if you have the funding."

New designs include programs such as the Air Force Dismount Detection Radar, says Dr. Paul Monticiollo, CTO at Mercury Systems in Chelmsford, MA. "We are also seeing radar and EW systems being moved onto UAV platforms. The F-16 and F-15E radar-modernization programs, where mechanically scanned arrays are being replaced by Active Electronically Scanned Arrays (AESAs). Enhancing the downstream signal processing is also a big part of these tech refreshes."

"Pretty much every company presenting or attending the Embedded Tech Trends conference in Phoenix in January 2014 listed radar as the key area for their signal-processing solutions."

Examples of programs that upgraded their radar signal-processing systems with Commercial-Off-The-Shelf (COTS) include the Raytheon Patriot Missile System radar and the Lockheed Martin AN/TPQ-53 (Q-53) counterfire target-acquisition radar. Designers of these systems like the high speeds of multicore processors such as the 4th-generation Intel Core i7 – also known as Haswell – high-performance FPGAs from Xilinx and Altera. For more on signal-processing trends, see my article in the Mil Tech Trends section on page 20.

"A lot of our radar business consists of upgrades to systems that are 15 or 20 years old," says Rodger Hosking, Vice President and co-founder of Pentek in Upper Saddle River, N.J. "Not only do our customers get improved performance with these upgrades, but they also see tremendous savings in total life-cycle costs because maintenance costs on older radar systems can be quite high."

Pretty much every company presenting or attending the Embedded Tech Trends conference (www.embeddedtech-trends.com) in Phoenix in January 2014 listed radar as the key area for their signal-processing solutions. In addition to the companies mentioned above, they include Kontron, 4DSP LLC, Vadatech, Elma, Alpha Data, CES, Artysen Embedded Technologies (formerly Emerson Network Power), AcQ, ADLINK, and Interface Concept.

We've also packed the issue with contributed articles from embedded computing companies, along with an article from Lockheed Martin on ISR as a Service on page 16. Our Mil Tech Trends section includes a piece from Cambridge Pixel on radar-display processing, another from Cypress Semiconductor on using high-performance SRAMs for signal processing, and one from Mercury Systems on signal processing for EW. In our Industry Spotlight section, Bittware and Curtiss-Wright Controls Defense Solutions penned articles on FPGA technology for use in radar and EW systems.

Budget cuts spur use of rugged COTS systems

By Charlotte Adams

A GE Intelligent Platforms perspective on embedded military electronics trends

As the U.S. defense budget shrinks, the military's appetite for rugged Commercial Off-The-Shelf (COTS) products will continue to grow. The services can no longer afford the protracted development schedules and massive cost overruns often associated with new programs. This makes COTS components – from chips to boards to subsystems and systems – attractive in every corner of the procurement world, especially for High Performance Embedded Computing (HPEC) in radar and other sensor applications.

COTS is attractive at the subsystem level because it can reduce risk levels of a program – especially cost and time to market – since there is no upfront Non-Recurring Engineering (NRE) overhead. Delivery time can be a matter of weeks and, because it is already ruggedized, the function takes less time to field. The subsystem, already packaged in a standard chassis, could serve as a platform for software development, interoperate as part of a larger system, or plug into a smaller platform at the system level after appropriate testing and certifications have been completed. Rugged COTS subsystems or systems typically have been tested in a laboratory, simulating the intended operating environment, and have achieved a correspondingly high Technology Readiness Level (TRL).

COTS technology can also reduce technical risks, from the early integration of cards, to analysis and testing of how well they work together, to interoperability with other systems, through operation and lifecycle support. Much work has been done upfront to ensure hardware compatibility and to fine-tune the operation of low-level software such as board support packages, drivers, and operating systems.

Ruggedness is also important. Although there is no overarching standard for this quality, vendors typically offer several levels of ruggedization – based on military specs – relating to prospective environmental factors such as temperature, shock, vibration, sand, dust, humidity, and saltwater corrosion. Products are often tested to procedures found in MIL-STD-810.

Figure 1 | The GE Intelligent Platforms D8I-3VF1 is a 3U VPX, forced air-cooled platform.

Ruggedization is now so common in military and aerospace products that it's typically considered from the beginning – from design, assembly, and test on through thermal management, mechanical engineering, and hermetic control. Ruggedization techniques include elements such as parts screening, substrate material selection, conformal coatings, stiffening, and cooling.

A rugged COTS system can offer a range of processing functions, such as generic CPU boards, video processing, and special-purpose signal processing cards with hundreds of processing engines per chip. But COTS also needs to be flexible, especially at the system level, where so many elements are provided that customers could literally be boxed in before they know it. It's important for the vendors to have built into their menu of architectures a wide range of flexibility, especially as to the I/O configuration.

An example of a rugged COTS subsystem appropriate for HPEC applications such as radar is the GE Intelligent Platforms D8I-3VF1, a 3U VPX, forced air-cooled platform with as many as three Intel multicore Core i7 boards expandable to eight slots, including video capture, General Purpose Graphics Processing Unit (GPGPU) and switch cards (see Figure 1). Its I/O capability ranges from MIL-STD-1553 and Gigabit Ethernet (GbE).

Increased demand

Rugged COTS subsystems and systems are becoming more common because the demand is growing. For example, U.S. Department of Defense (DoD) spending for COTS-equipped aircraft, such as the P-8 Sub Hunter and the KC-46 Tanker, reached $4.71 billion in 2012 and will spike between 2013 and 2016, as these programs reach full production, according to Frost & Sullivan, a U.S. market analysis firm.

Revenues for unmanned systems – which leverage rugged COTS technology and put a premium on ruggedization, as well as economies of Size, Weight, and Power (SWaP) – are expected to grow even faster. The aviation side of this market could grow at an annual 12 percent compound annual growth rate, hitting $18.7 billion in 2018, say analysts at Market Research Media. That could produce $86.5 billion in revenues from 2013 to 2018. These numbers don't include the proliferation of civilian Unmanned Aerial Vehicles (UAVs), which recently received the blessing of the U.S. Congress. Civilian UAVs will also be deployed with COTS systems.

The military clearly wants more economical and less time-consuming solutions, and rugged COTS is a proven approach to this end.

defense.ge-ip.com

Latest 40 Gbps SBCs drive new class of HPEC-Lite systems for ISR applications

By Alan Baldus

An industry perspective from Curtiss-Wright Controls Defense Solutions

The embedded defense and aerospace industry has recently seen the emergence of new embedded system elements that support 40 Gbps fabrics. These higher bandwidth hardware solutions include Single Board Computers (SBCs), DSP engines, GPGPUs, FPGA engines, network switches, and Gen3 OpenVPX backplanes. With their support for 40 Gigabit Ethernet (GbE) and QDR Infiniband (for board-to-board communication) and Gen3 PCI Express (for on-board data flows), these system elements enable the integration of large-scale rugged embedded subsystems that approach supercomputer processing levels. These high-end processing systems can now address challenging Intelligence, Surveillance, and Reconnaissance (ISR) applications in low- to mid-range systems with three to five boards in a small, compact chassis.

System designers can now use the latest generation of SBCs that feature dual channels of 40 Gbps bandwidth and support for 3rd Gen PCIe-enabled XMC mezzanine module sites to define a new class of entry-level "HPEC-Lite" systems. With their higher 40 Gbps bandwidth, the latest SBCs can now serve as dual-use platforms in small low- to medium-level High Performance Embedded Computing (HPEC) systems, providing both their traditional system management functionality and the high-speed data ingress functionality that previously required the use of a dedicated, but lower speed, XMC I/O carrier board in an ISR HPEC system.

Small HPEC systems such as the Curtiss-Wright 6U VPX6-1958 board bring in analog front-end data to the board via its high-speed I/O XMC mezzanine cards at PCI Express (PCIe) rates (see Figure 1). The raw captured data is then sent directly from the SBC at 40 Gbps rates to one or more DSP engines for ISR application processing. This "HPEC-Lite" approach eliminates the need for a slower, PCIe-based XMC carrier card and the dedicated board slot it would require. Instead, the SBC functions as a high-speed intelligent router that can run a TCP/IP stack to support a redundant 40 GbE data pipe to the system's DSP engines. Via its dual/quad 40 Gbps pipes, Core i7 CPU, and high-speed XMC sites, the SBC becomes a high-end sensor I/O distribution subsystem.

Figure 1 | Curtiss-Wright's VPX6-1958 board, which uses the latest Intel 4th Generation Core i7 processor and dual XMC sites, enable HPEC-Lite systems for SWaP constrained ISR applications.

The SBC's Intel 4th Generation Core Haswell processor, with its built-in GPU, can deliver unprecedented levels of performance – 300 GFLOPS from either the CPU or GPU, which combined brings more than 600 GFLOPS of performance from a single Intel processor. In an HPEC-Lite system like the one mentioned above – with a lone VPX6-1958 SBC and two DSP engines, the result is >2 TFLOPS of processing performance. This performance is expected to increase, as future Intel processors are anticipated to enable 4 TFLOPS in a similar 3-board small HPEC system.

Many ISR applications will continue to require larger board sets. However, the compact HPEC-Lite approach will enable many types of ISR applications with low Size, Weight, Power, and Cost (SWaP-C) requirements, to be solved with a small deployed chassis. For example, a radar-processing system can be built using the smaller system to bring in raw data at the front-end via Serial FPDP (sFPDP) via the SBC's XMC cards, and then transfer that raw radar data with minimal latency to one of the system's two DSPs for post processing.

Another potential application is visualization data processing, particularly when pattern matching is required in unmanned aerial vehicles, ground combat vehicles, and airborne sensor pods. In this type of application the SBC's XMCs would use the XF05 camera link digital video-transmission standard to bring the raw video data to the small HPEC system, which would then route the data to the system's DSP engines for post processing.

In this dual-use approach, the SBC is still able to provide the traditional "traffic cop" system management functionality, but now also acts as the ingress system for the front-end data, sending raw data via PCIe to dedicated GPGPUs, or via 40 Gbps fabrics to DSP engines. For those ISR applications that require the greatest processing power and performance possible, 40 Gbps end-to-end system elements enable the development of large "big iron" scalable HPEC systems that can move terabytes of data. Yet, these high bandwidth board elements also enable designers to address less demanding applications with low- to mid-level subsets of those solutions, saving space, weight, power, and cost.

Alan Baldus
Product Marketing Manager, Intel SBCs
Curtiss-Wright Controls
Defense Solutions
www.cwcdefense.com

DEFENSE TECH WIRE

NEWS | TRENDS | DOD SPENDS | CONTRACTS | TECHNOLOGY UPDATES

By Amanda Harvey, Assistant Editor

NEWS

Rocket-based weapon system demonstrated for small ship protection

Engineers at Raytheon and L-3 Communications fired Raytheon-made TALON laser-guided rockets from a L-3 remote weapon station (designed by L-3) using an LAU-68 launcher. The test demonstrated how small ships can be protected by using the lightweight remote weapon system integrating the already-fielded launcher and sensor systems as well as the TALON missiles.

The system, which can carry as many as seven TALONs uses an electro-optical sensor and laser designator, for a total weight of about 500 pounds. It only needs a target queue for engaging on-mount target tracking and can be used on ships ranging in size from riverine to a major surface combatant. TALON is a cooperative development program between Raytheon and the United Arab Emirates.

Figure 1 | The Raytheon TALON laser-guided rocket were fired from a L-3 remote weapon station using an LAU-68 launcher. Photo courtesy of Raytheon.

Frost & Sullivan predicts U.S. DoD Special Operations Command spending to stabilize through 2018

Analysis from Frost & Sullivan's U.S. Department of Defense (DoD) Special Operations Command (SOCOM) budget shows $10.09 million was spent on military products and services in 2012, and is expected to reach $10.60 million by 2018. The spending is anticipated to remain stable during the next four years, in spite of current budget concerns.

Frost & Sullivan also predict investments in Commercial Off-The-Shelf (COTS) products and networking tools will rise as costs are lowered and efficiency enhancements are made. In the next four years, the U.S. DoD SOCOM is also expected to spend on new platforms, including Ground Mobility Vehicles (GMVs) and training. In terms of technology, spending will primarily focus on Size, Weight, and Power (SwaP) product improvements. Analysts also predict that command and control; communications; computers; Intelligence, Surveillance, and Reconnaissance (ISR) systems; rotary-wing applications, and training and simulation programs will increase exponentially.

Software and hardware on Marine Corps AN/TYQ-23(V)4 command, control and communications TAOM getting upgrade from Northrop Grumman

Northrop Grumman won a U.S. Marine Corps contract to deliver post-production life-cycle support for Marine Corps AN/TYQ-23(V)4 Tactical Air Operations Module (TAOM) and related subsystems through fall 2014. Under this new contract, Northrop Grumman engineers will work to sustain and upgrade the circuit card assemblies, hardware, and software of the command and control systems that support the TAOM. Software improvements will also be made to the Multi-Radar Tracker and Data Communications Unit.

The system is a transportable command, control, and communications facility that operates in conjunction with the AN/TYQ-87(V)2 Sector Anti-Air Warfare Facility and its peripheral equipment for surveillance, threat evaluation, identification, weapons coordination, communications capabilities, and airspace management. Each TAOM contains mission-essential equipment such as computers and digital voice communications systems that are required for command and control functions.

Top Secret NSA certification given to TacNet Tactical Radio from Rockwell Collins

The TacNet Tactical Radio (TTR) from Rockwell Collins in Cedar Rapids, IA, garnered final National Security Agency certification to Top Secret. The TTR enables Link 16 networked communications to new users.The small form factor radio has a selectable power output with 1-, 50-, and 90-watt transmission modes; increased range; and free air convection cooling allowing it to adapt to any warfare environment. TTR provides a common operating picture through Link 16 networked communications.

Applications for TTR include unmanned aerial vehicles, rotary-wing aircraft, military vehicles, forward air controllers, and mobile and transportable ground stations as well as small maritime assets that have not had access to Link 16 capability in the past. Link 16 also integrates command and control data including the sharing of targeting and situational awareness data among joint and coalition partners. TTR has a volume of less than 185 cubic inches and weighs less than 10 pounds. For more information, visit www.rockwellcollins.com/ttr.

Figure 2 | The TacNet Tactical Radio (TTR) from Rockwell Collins received Top Secret NSA certification. Photo courtesy of Rockwell Collins.

WHITE PAPER

Thermal management challenges and solutions for avionics systems

By: Mentor Graphics Corporation

The main source of heat in electronic equipment is their semiconductor chips, and the temperature sensitivities of these chips presents a challenge in designing cooling mechanisms. Overheating causes the chips to prematurely fail, and failure of only one chip can disable the entire equipment. The higher the chip temperature, the earlier and more certain the failure. As functionality has increased, the associated heat dissipation has escalated to the extent that it is recognized as a potential limitation on the pace of electronics development. Appropriate cooling strategies are needed to prevent overheating and failure of critical components. This white paper addresses thermal design challenges for electronic products.

Read the white paper: http://opsy.st/1e3Y9Ec

More white papers: whitepapers.opensystemsmedia.com

E-CAST

Enabling open architectures in rugged ISR: Innovation in radar and electronic warfare systems through signal processing

Presented by: GE Intelligent Platforms, Mercury Systems, Pentek, and Thermacore

Gaining the tactical edge on the battlefield is becoming less about troop and tank deployments but more about who has the smartest sensors, best Electronic Warfare (EW) techniques, and the most accurate radar systems.

As the U.S. defense budget shrinks and the military reduces its global footprint, funding for these applications remains steady, even increasing in some programs. According to Frost & Sullivan radar contracts increased from a value of $3.27 billion in 2011 to $4.26 billion in 2012. The increased demand also places more pressure on system performance, driving innovation at the signal processing level so radar and EW systems can track every target and every signal. Often this performance is found in commercially developed, embedded signal processing components in open architecture designs. This webcast of industry experts will discuss how EW and radar system designs leverage these components and overcome challenges such as reduced Size, Weight, and Power (SWaP) requirements.

Register for the free e-cast:
http://ecast.opensystemsmedia.com/445

View archived e-casts:
http://opensystemsmedia.com/events/e-cast/archive

E-CAST

Maximizing system performance in time and space partitioned DO-178 certifiable safety-critical systems

Presented by: DDC-I

ARINC 653 Part 1 (653p1) defines a standard Real-Time Operating System (RTOS) Application Executive (APEX). It provides partitioning and a relatively simple, standards-based API, which facilitate porting and reuse of 653 applications.

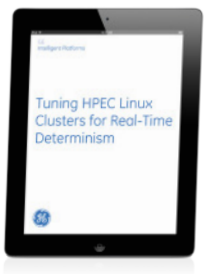
Priority-preemptive RTOSs offer flexible scheduling models, which allow efficient scheduling of more complex applications. However, very few of these RTOSs support guaranteed execution of tasks, also known as time partitioning.

Merging these two models into a hybrid solution offers the best of both worlds: standards-based commonality and advanced features that can yield the highest performance possible for safety-critical software operation. Industry experts from DDC-I will highlight RTOS technology that allows developers to merge these two approaches into a hybrid model, and will discuss the resulting benefits.

Register for the free e-cast here:
http://ecast.opensystemsmedia.com/447

View upcoming e-casts:
http://opensystemsmedia.com/events/e-cast/schedule

WHITE PAPER



Tuning HPEC Linux clusters for real-time determinism

By: GE Intelligent Platforms, Inc.

This paper investigates interrupt response times and message passing latencies using OpenMPI on three different versions of the Linux kernel: one "standard" server grade, one server grade with real-time pre-empt patches applied, and one with a proprietary, real-time kernel. In order to characterize these platforms, a series of measurements were made with and without a background CPU load.

This paper will also highlight some system and Linux kernel tuning techniques that can improve determinism and affect system performance. The results are presented in a series of graphs showing histograms of interrupt response and MPI message latencies under the various workloads and tuning scenarios.

Read the white paper: http://opsy.st/1klogn5

More white papers: whitepapers.opensystemsmedia.com

New capabilities on the way for airborne maritime surveillance radars

By Sally Cole, Senior Editor

Airborne maritime surveillance radars play a central role in the global homeland defense of more than 315,000 miles of worldwide coastline. While considered state-of-the-art, these radars continue to evolve to meet military customers' needs for persistent surveillance, automation, and continued tracking of targets as they move from sea to land.

Maritime radars are often used in Unmanned Aerial Vehicle (UAV) platforms such as the U.S. Customs and Border Patrol's Guardian. Photo courtesy of Raytheon.

From a mission standpoint, the traditional role for airborne maritime surveillance radars was anti-surface warfare, or basically detecting small targets on the ocean surface in heavy sea states. This capability was critical during the Cold War, at a time when the US Navy needed to quickly detect small targets such as Russian periscopes.

After the Cold War, the land-sea border known as the littoral zone has emerged as an area of intense interest. Within the littoral zone, the challenge for airborne maritime surveillance involves looking at thousands of targets in the water because anything floating on the surface – including debris and trash – appears as a target. This can make it challenging for radar operators and mission commanders to quickly make sense of a complex tactical picture and zero in on actual targets.

Industry leaders Telephonics Corp. (Farmingdale, NY; www.telephonics.com) and Raytheon (McKinney, TX; www.raytheon.com) are addressing the littoral zone issue and many other challenges by continuing to enhance the capabilities of their airborne maritime surveillance radars.

Capabilities requested by military customers

What types of capabilities are military customers requesting for airborne maritime surveillance radars today? For starters, airborne maritime surveillance radar used in a military application must be military grade and able to survive the airborne environment.

"For maritime surveillance, one of the key capabilities is the ability to detect small targets at long ranges in heavy sea states," says Joseph Battaglia, president and CEO of Telephonics Corp. "Heavy seas can obscure relatively small targets, so it's important to know how to extract the target of interest from the background sea clutter, which interferes with the ability to detect the target."

The military often needs to identify targets of interest, and Inverse Synthetic Aperture Radar (ISAR) imaging is one of Telephonics' strengths. "Telephonics' images have been referred to as 'eyewatering,' because of their high resolution and crispness. These images can help identify a battleship from a cargo ship from a pleasure yacht. Whatever the target is, you'll see a physical image of it on the radar display, as opposed to the classic radar return, which would be a dot on the screen," Battaglia says.

Military customers also want to detect targets with an Identification Friend or Foe (IFF) capability. IFF systems are typically separate systems on a platform. "Telephonics has fully integrated the IFF function into our radar systems, which along with saving size, weight, and wiring on aircraft, actually performs better than two separate systems that are required to communicate," Battaglia says.

Yet another important capability? The Ocean Surveillance Initiative (OSI), in which the automatic identification system (AIS) works with the OSI to provide a complete operating picture of the field of regard.

Adding OSI and AIS functions to maritime surveillance radars "enables persistent surveillance and a littoral capability, providing the operator a common operating picture (COP)," Battaglia explains. "Submarines are probably the worst threat to the fleet. Some of Telephonics' radars provide a periscope detection mode and are deployed on fixed-wing aircraft, helicopter platforms, and UAVs [Unmanned Aerial Vehicles] to ensure the fleet is well protected." (See Figure 1).

As part of Raytheon's recent XMC (eXpanded Mission Capability) upgrade to its SeaVue radar, the company enhanced its radar system to automatically correlate radar and AIS tracks. "The radar presents a single track to reduce clutter on the display and provide additional information to the operator," says Brad Hopper, business development director in Raytheon's Intelligence, Surveillance, and Reconnaissance systems mission area.

Although AIS is typically on larger ships – 300 tons or more – this capability is particularly useful if a small target is being tracked in a shipping lane with lots of large ships. With the click of a button, according to Hopper, the operator is able to remove those larger targets from the display and concentrate on the target of interest.

Out of concern about hijacked ships spoofing AIS, the Raytheon radar can provide an automatic length estimation of radar-detected ships. "If you're far enough away and can't get eyes on with electro-optics, now you can check it against the length AIS is sending to protect against spoofing," Hopper says.

Persistent surveillance's influence on radar design

Persistent surveillance is influencing the design of airborne maritime surveillance radars in several ways, in particular, automation.

"Historically an operator spent more time operating the radar than understanding what's on the surface of the ocean. A significant amount of automation was added during Raytheon's XMC upgrade to SeaVue to help out in this area," Hopper notes.

For example, if you have a critical piece of infrastructure such as a power plant or oil platform and don't want anything (such as a vessel) getting close to it, you can use SeaVue XMC software to set up an exclusion zone so the operator is automatically alerted if anything moves in or out of it. "This ability to automate the process and help the operator understand what's happening in the littoral environment is significant. Customers say this capability with SeaVue XMC has reduced their operator workload by 50 percent, so now they can spend time doing the real mission and not just operating the radar," Hopper says.

Figure 1 | The AN/APS-153(V) maritime radar from Telephonics Corp. is found on the U.S. Navy's MH-60R helicopter. Photo courtesy of Telephonics.

Being able to do precision tracking on each one of these targets also enables persistent surveillance. "One of the problems with long-term surveillance of a certain area is that small targets of interest tend to lump together and targets that are trying to hide from you will purposely get into a fishing fleet or cross into a transit lane to avoid detection," Hopper adds. "We've added precision tracking into the SeaVue XMC to help with persistent surveillance and to ensure we maintain track on that target no matter how small it is or how it's maneuvering."

Leveraging COTS signal-processing solutions

Are new airborne maritime surveillance radar systems leveraging Commercial-Off-The-Shelf (COTS) signal-processing solutions to meet performance requirements and enable open architecture designs? Absolutely.

Telephonics' technology tapped for US Navy UAVs

Telephonics Corp. (Farmingdale, NY; www.telephonics.com) has differentiated itself in the airborne maritime surveillance radar market by developing a technology that uses smaller, lighter-weight transmitters, which don't require high-voltage power supplies.

"Since the late 1950s, Telephonics has focused on extracting targets from background sea clutter. Our front-end designs, waveforms, algorithms, signal processing, and software are optimized for maritime surveillance," explains Joseph Battaglia, president and CEO of Telephonics.

Telephonics' RDR 1700B, or AN/ZPY-4, has no real competitor for a radar of its size, weight, performance, and price, according to Battaglia. "We believe it's unique in the world, and its application to rotary or fixed-wing platforms – including UAVs – is ideal. Weighing in at 68 pounds, its imaging, integrated AIS and OSI, and small-target detection performance at operational ranges is unique in the industry," he says.

Telephonics is providing the radar for Northrop Grumman's (Falls Church, VA; www.northropgrumman.com) MQ-8B Fire Scout, a rotary-wing UAV, which will be deployed soon.

"As far as signal processing is concerned, there are many COTS solutions you can buy off the shelf," Battaglia says. "High-speed, high-throughput processors are used to accomplish the system performance we desire. The key to achieving the requisite performance is primarily driven by the algorithms and software embedded on these processors. Telephonics' algorithms are optimized to differentiate between sea clutter and targets."

Raytheon also takes advantage of high technology in the commercial world whenever it can for its radar products. "Some of Raytheon's airborne maritime radars use COTS products, such as the Freescale PowerPC G4," Hopper says. "In this case, these are put onto a ruggedized board by a supplier like Mercury Systems, and then we buy the board. We use this kind of processor because as they improve, we want to be able to upgrade without major impact to customers."

However, "you should use care when selecting COTS components for this application because they need to be able to survive the fairly severe environment of an airborne platform," Hopper cautions.

New capabilities on the way

Expect the trend toward reducing size, weight, and power consumption for airborne maritime surveillance radars to continue, but also watch for other interesting capabilities to emerge within the next few years.

Raytheon is currently is adding a ground-moving target indicator (GMTI) capability, based on demand from international customers. For homeland security missions, for example, if you're tracking someone bringing illegal drugs in on a vessel, you can track them right up the coastline, but then they can transfer cargo to a truck and just drive away – the maritime mode can't continue to track them. "GMTI mode will enable continued tracking, so you'll be able to get land forces vectored there to intercept them," Hopper says. "Raytheon will demonstrate GTMI capabilities for SeaVue XMC during 2014."

Active Electronic Scanned Array (AESA) radars using conformal antennae offer next-generation capabilities for maritime surveillance. Rather than using a rotating antenna, there are a number of ways to implement AESA radar onto a platform – in the nose of the craft, under the belly, or incorporated into the aircraft's skin as a panel.

"AESA designs eliminate moving parts, increase reliability, and offer 'graceful degradation' of a system when failures occur," Battaglia notes.

It may be a while, however, before AESA technology is ready to compete in the airborne maritime radar market with other systems for the same size, weight, performance, and price point. High-performance AESA systems tend to be significantly larger and can be liquid cooled, which makes them bulky and expensive – but this is all likely to change at some point in the future. MES

SynQor

Uninterruptible Power Supply

Rugged

Smaller

Lighter

More Powerful

- **Power: 1250W/1500VA**
- **Weather-proof, shock-proof construction**
- **True on-line double conversion**
- **1U high rack mount (17" x 22" x 1.73")**
- **Low weight — 32 pounds**
- **Dual input (AC and DC)**
- **Battery run time >10 minutes**
- **Removable battery pack**
- **Full power operation: -20 °C to +55 °C**

Made in the United States of America.

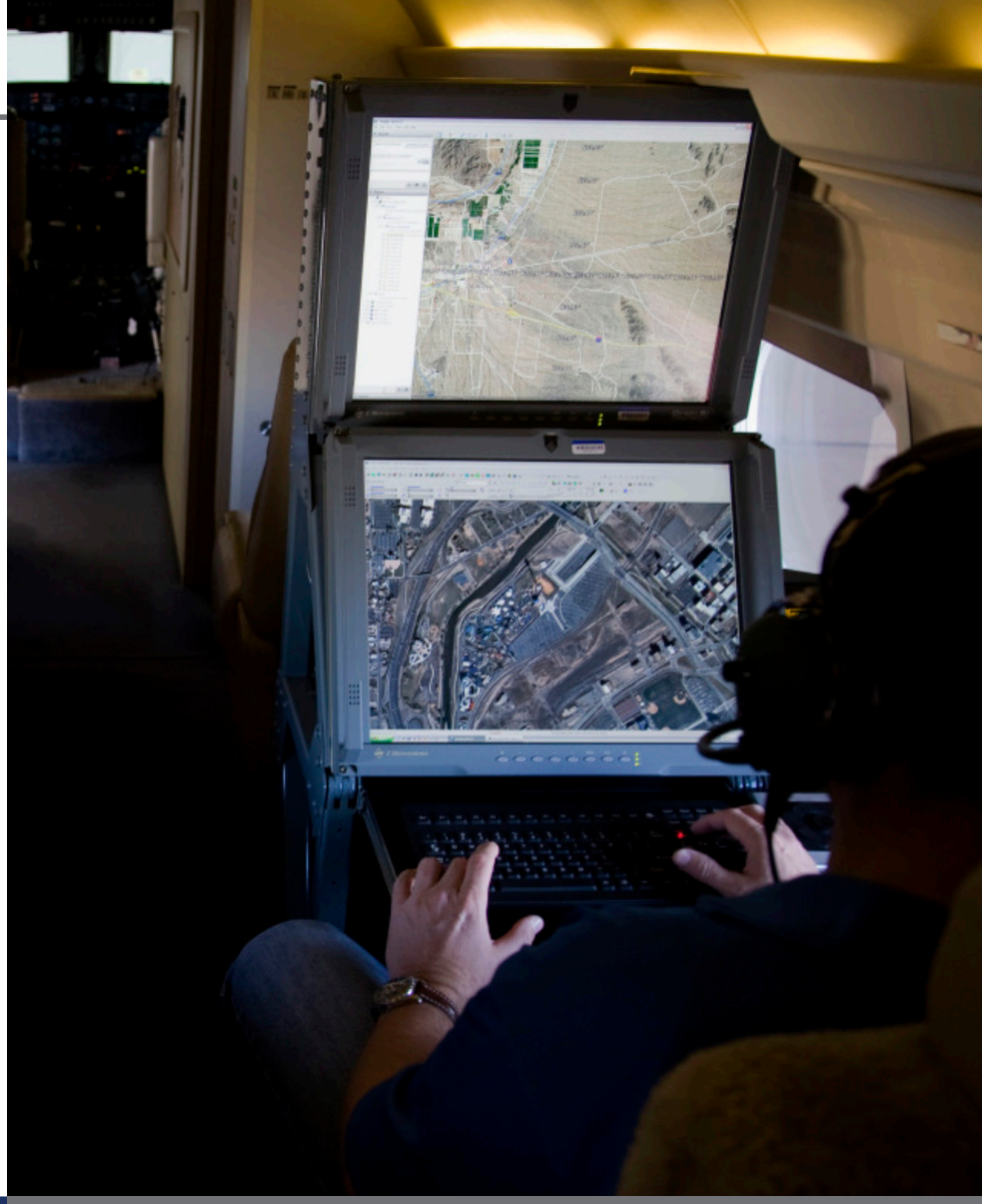
1-978-849-0600 www.SynQor.com

SynQor®

ISR as a Service: Providing users with affordable surveillance and reconnaissance

By Robert Smith

As the type and number of military and national security threats increase, so does the sophistication and capabilities of Intelligence, Surveillance, and Reconnaissance (ISR) systems needed to address those threats. The problem, however, is that developing and operating advanced ISR systems is costly, and in many cases a user does not have the time, resources, acquisition processes, or technological maturity to make an ISR procurement practical.



Lockheed Martin designed its Airborne Multi-INT Laboratory (AML) with an open architecture so that a myriad of intelligence-sensor combinations can be easily integrated and interchanged into the aircraft's mission system.

One of the many challenging realities of today's evolving landscape of threats is that nations, alliances, and organizations with great need for sophisticated ISR capabilities often find it difficult to develop, field, and operate those capabilities. Perhaps they lack the budget resources to procure an ISR platform or have no acquisition group available to efficiently procure such a sophisticated system. They may not have a mature ISR organization to operate the collection system, or the luxury of time to wait for the implementation of a system. For these entities, the answer lies in ISR as a Service, or ISRaaS. By procuring the specific capabilities it needs to fulfill specific mission objectives – whether they are military, homeland defense, or even disaster relief and humanitarian assistance – this type of customer can rapidly fill the gaps in its ISR capabilities according to its situational requirements.

This approach to solving a user's ISR limitations brings its own set of challenges. Because of the high variability of each user's circumstances, each solution must be customized and configured to align with a unique combination of a user's resources, organizational maturity, mission requirements, and potential export restrictions. This need for customization might, in theory, appear to undermine one of the fundamental benefits of the service model, which is the cost effectiveness realized from standardization and reuse. In practice, however, the challenges can be overcome through a modular hardware and software architecture that supports highly adaptable technology solutions combined with technical and operational expertise.

Defining the ISR user's need – and solution

The first phase in a successful ISRaaS implementation is fully defining and understanding the ISR user's problem set. This approach has some of the characteristics of a commodity, in that it seeks to offer highly capable yet cost-effective solutions by applying standardized components to a task or set of tasks. Other features, however, are more characteristic of a development program, in that the components often require a high degree of customization and, therefore, close attention to mission definition and systems integration.

It is imperative that an ISRaaS provider focuses on helping each user determine the precise nature of the capabilities that address the mission, fit their available budget, and satisfy their overall

> Modern system design, which collects metadata associated with all aspects of the system, is a great advantage, as compliant metadata formats are required to facilitate content discovery queries.

Figure 1 | In Lockheed Martin's palletized Dragon Shield configuration – for users who need to perform multiple missions such as airlift and ISR – the ISR sensor and processing systems are built onto pallets or trailer-like containers that can be rolled on and off aircraft.

ISR goals. Take, for example, a NATO member with a need for expeditionary ISR capabilities. This user has an existing ISR infrastructure and skilled operators and analysts, but its procurement budget is insufficient to acquire a new platform. In this case, they may be best served by a service-oriented solution that provides a multi-intelligence, contractor-owned airborne ISR platform and ground processing systems. The aircraft is piloted by the contractor, but the onboard mission system, ground system, and data are controlled entirely by the ISR user. If and when they are ready to purchase the capability, the user's operational experience will have greatly influenced the final requirement set, and thus reduced any procurement risks.

On the other end of the scale, in the simplest form of ISRaaS, a user may go with a contractor-owned, contractor-operated capability where the data gathered by airborne sensors – perhaps small aircraft or even an aerostat – is passed directly to the user via live data feeds and may be recorded for later processing. With the contractor in full control of sensor cueing and data gathering, this arrangement relies on close communication to identify the user's collection requirements.

In a third category, the ISR user may have a need for advanced ISR capabilities and a willingness to purchase a platform, but no desire to develop an infrastructure of analysts and processing capabilities. In this case, they may choose an ISRaaS solution that covers only the processing, exploitation, and dissemination portion of the ISR capability.

ISRaaS platforms can come in all shapes and sizes to fit user needs. Maintaining synergies with existing sovereign assets can eliminate infrastructure changes; evaluating a new philosophy by changing asset type (such as an aerostat) can help develop techniques and training for a potential future procurement; and utilizing a roll-on, roll-off containerized ISR suite carried by an existing multipurpose airlifter – as seen in Lockheed Martin's Dragon Shield in Figure 1 – can enhance the value of an existing platform and avoid the cost of an additional aircraft.

Interfacing with a user's C2 and ISR enterprise

When the problem set and best-value solution are determined, the next challenge is implementing the interfaces and data-format compliance between the ISR system and the customer's network or networks. Nations, alliances, and organizations are understandably protective of their data-network security, yet ingesting ISR data requires exposing a number of interfaces to those networks. The first steps to making that happen include designing the ISRaaS-enabled architecture with a minimum of unique interfaces, and ensuring standardization of the data that will be transferred across those controlled interfaces.

Applying the appropriate data adapters requires very little development in most cases, especially for systems that are fully compliant with published standards. Adding to the challenge, however, can be the many available types of sensors, data streams, and customer processing systems. Depending on the user, the data feeds may include standard- and high-definition video, still images, signals intelligence (SIGINT), and others. Data may be collected from a number of sources, including electro-optical and infrared imagery, synthetic aperture radar, and Moving Target Indicators (MTI) for ground, air, maritime, and dismounted targets.

All of the various sensor outputs can be recorded as well as streamed from the platform to the ground system through a data link. Additionally, if sensor outputs are to be ingested by the end-user for further exploitation, they must be adapted to ensure compatibility in that environment. This could be as straightforward as providing standard-definition video to which a desktop user can subscribe and display in a browser, or it could take more complex forms if the data from all intelligence domains is to be ingested and processed.

Modern system design, which collects metadata associated with all aspects of the system, is a great advantage, as compliant metadata formats are

required to facilitate content discovery queries. A sophisticated ISRaaS solution enables operators, whether they're sitting in a mobile ground station or in an aircraft, to perform federated queries across metadata catalogs for all intelligence domains and locations. Recent developments are greatly improving the ease with which varied intelligence products can be integrated, queried, and displayed.

Another consideration is the sharing of data with coalition forces. NATO members, for example, adhere to a range of standardization agreements that define the way video and metadata is encoded over a network. Properly encoded data can be shared through a coalition shared database. An ISRaaS user could, for instance, capture still imagery from a streaming feed and post it for coalition partners using NATO Secondary Imagery Format without additional processing. NATO customers are then able to engage in a higher level of data sharing and interoperability with systems that participate in NATO's Joint ISR planning and operations as demonstrated in Unified Vision exercises. It is critical to remember, however, that when the platform is integrated with national, coalition, or alliance elements, designing how data flows throughout the system is a key early task.

Future of ISRaaS

Clearly, the need for ISR capabilities continues to grow around the world as entities of all kinds seek to protect their borders, assets, and population. When acquisition cost, timeline, or technical expertise is a limiting factor for a user, ISRaaS is often a viable alternative. It enables the rapid deployment of intelligence capabilities, using a range of deployment models tailored to each user's circumstances, providing superior value for money and critical operational effectiveness for them.

Lockheed Martin is providing ISRaaS systems to a number of users via its "Dragon" family of ISR configurations that are used for various missions. The Dragon Dome, as seen in Figure 2, links ISR, air operations, and missile defense;

Figure 2 | Dragon Dome links ISR, air operations, and missile defense systems at the battle-management level, enabling users to work together in a shared environment to optimize defense operations.

Figure 3 | A flying laboratory, the AML – also known as Dragon Star – is a used business jet that Lockheed Martin engineers modified into a flying test bed for testing and fielding C4ISR capabilities. The Dragon Star configuration addresses requirements for midrange, multi-intelligence platforms such as the Gulfstream III, Havilland D-8, or Beechcraft B350, all of which can be equipped with a variety of sensor and communications systems.

while the Dragon Star flying laboratory (see Figure 3) serves as an airborne test bed for C4ISR capabilities. **MES**

Robert Smith *is vice president of C4ISR Systems for Lockheed Martin Information Systems & Global Solutions. He leads a comprehensive portfolio of Command, Control, Communications, Computers, Intelligence, Surveillance, and Reconnaissance (C4ISR) programs. In this capacity, he is responsible for more than 100 programs that provide services and capabilities for all branches of the U.S. military, various national agencies, and numerous international customers. Smith received a bachelor's degree in chemical engineering from the University of Maryland, a master's degree in business administration from Johns Hopkins University, and a doctoral degree in chemical engineering from Auburn University.*

Lockheed Martin Information Systems & Global Solutions
301-897-6230 • www.lmco.com

DRAGON

it's not a myth.

- Rugged PC/104 enclosure
- Data acquisition
- Monitoring • Recording
- MIL-STD-1553/1760
- AS5652 (MMSI) • H009
- ARINC-429/575 • ARINC-708
- CANBus • A/D • D/A
- Serial • Discrete
- User configurable
- COTS • Expandable
- Extreme environments
- Accepts third party cards

EXCALIBUR SYSTEMS

www.mil-1553.com

CAMELOT MACC LANC

Embedded signal processing enables advanced radars and EW systems with low latency

By John McHale

GE's XVR16 6U VME rugged single board computer uses the Haswell 4th generation Corei7 processor from Intel.

Modern radar and electronic warfare designs rely heavily on embedded computing systems that leverage high-speed commercial processors and FPGAs to find every target or signal and enable the warfighter to respond in real time. Meanwhile, signal processing system designers are cutting costs by using parallel compute platforms such as OpenCL that work across multiple chip platforms.

The basic premise of Moore's Law – that the performance and speed of integrated circuits doubles about every six months to two years – mirrors the computational demands of modern radar and Electronic Warfare (EW) systems that have ever-increasing performance requirements. Radar programs need to track sophisticated missiles and find targets in high-noise environments, while EW system designers are pressured to track all signals while remaining undetected by a sophisticated enemy. Clever algorithms drive these EW and radar platforms, but they need the right mix of commercial GPUs, multicore processors, and FPGAs to perform wonders at the sensor level.

Rugged embedded computing systems that leverage these components in low Size, Weight, and Power (SWaP) solutions enable this innovation throughout the sensor chain. Just as military program managers strive to improve the kill chain in modern weapon systems by shortening the time from sensor to shooter, radar and EW designers are similarly looking to tighten integration along different parts of the Intelligence, Surveillance, and Reconnaissance (ISR) sensor chain to improve not only precision in data acquisition but also to deal with latency challenges. Engineers at Mercury Systems in Chelmsford, Mass., say the chain consists of six parts – acquisition, digitization, processing, storing, exploiting, and dissemination through electronic countermeasures.

"Where I see the greatest levels of integration effort is in the sensor chain, where you couple RF stages with mixed signal acquisition and digital processing stages," says Marc Couture, Director of Product Management at Mercury Systems. "The sensor chain stages are all about capturing the real world with an aperture, zooming in a target window in the electromagnetic spectrum, and presenting as much fidelity as possible to an analog-to-digital converter. This is how you know that your digital representation of the real world is as accurate as possible. Then your compute elements can go to work on the 1s and 0s."

"We can expect advances in electronics to enable tighter integration of current EW subsystem components," says Dr. Paul Monticiollo, CTO of Mercury Systems. "For example, as opposed to having separate 'boxes' for receivers, digital RF memory, signal processors, and threat managers, we expect to see a consolidation trend that will not only yield improved performance but also reduced long-term maintenance costs."

Demand is constant for more speed and more density and array type products, to process all the data being acquired, says Jenny Donaldson, President of Annapolis Microsystems in Annapolis, Md. Program managers are looking toward embedded Commercial-Off-The-Shelf (COTS) systems such as OpenVPX radar, airborne telemetry, synthetic aperture radar, and signals intelligence – anything that needs fast processing, Donaldson says. Annapolis offers the WILD OpenVPX EcoSystem that mixes and matches FPGA-based COTS OpenVPX boards.

Improving latency

"In EW systems minimizing latency is very important," Mercury's Monticiollo continues. "Missiles move extremely fast and there is not a lot of time to react and apply a countermeasure. Systems will have to be able to operate more autonomously in case communication links are jammed. For that you will need the signal processing to have a tighter degree of interaction with the mission computer – communicating between different functions and maybe even having the mission computer integrated with signal processor. Advances in SOC designs will help this and once we have these new capabilities in the circuit world we can think about how to design new systems."

"Low latency will be enabled by increased fabric speeds underneath individual boards and processors," says David Jedynak, CTO at Curtiss-Wright Controls Defense Solutions in Ashburn, Va. "The low latency requirements are pushing the move toward fabrics such as Infiniband or 40 Gigabit Ethernet, so you can move data without a lot of processor overhead. Curtiss-Wright is involved in the 40 Gigabit Initiative to provide 40 gigabits per second performance in systems from end to end."

"The biggest thing that's made a difference for us was the introduction of GPUDirect, which solved one of the challenges in using GPGPUs regarding latency in sensor data," says Peter Thompson at GE Intelligent Platforms in Huntsville, Ala. "Previously you'd take a signal across PCI Express to the Intel processor to memory and then send it to the GPU, which takes extra time and creates extra latency. With some EW applications those extra nanoseconds make a world of difference because you have a finite time to gather the signal and react. GPUDirect is a piece of technology that enables you to send sensor data straight across PCIe directly to the GPU." GE offers the XVR16 6U VME rugged single board computer for signal processing applications. (See Figure 1).

Fast FPGAs on front end

Reducing latency is also enabled by modern FPGAs on the front end of designs, where they process algorithms at very high rates. "FPGAs are front and center as the first signal processing element for our radar customers," says Rodger Hosking, Vice President and co-founder of Pentek in Upper Saddle River, N.J. "What they are doing with radar is trying to enhance detection range, bring more resolution to the front end, etc. This all ties into getting higher resolution on the de-converters, which ties into the ability to achieve higher precision with the radar detection algorithms, so they can detect smaller targets that have weaker signal levels. They want to track the targets that are buried in noise with these algorithms and the de-converters can pull those signals out. Another thing FPGA technology enables is target classification and identification by helping correlate vehicle signatures with a known database of targets – figuring out who to whom each signal belongs."

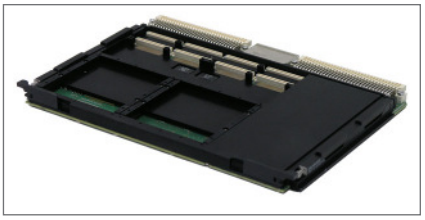


Figure 1 | GE's XVR16 6U VME rugged single board computer uses the Haswell 4th generation Corei7 processor from Intel.

"There is innovation coming with the next generation of FPGAs," Monticiollo says. "They are extremely more powerful with microprocessors being built in and heading toward true System-on-Chip (SoC) designs. High-performance FPGAs, microprocessors, and multicore processors can all be integrated on the same die, which will reduce latencies to microseconds and even nanoseconds for some applications."

"FPGAs are good at processing wideband radar signals in real time," Hosking says. "They are better than general-purpose processors (GPPs) They are better than GPPs in this instance because of the data rate. For example, radar systems can have as many as 48 lines running at 900 megahertz each and the only animal that can that is an FPGA. They enable flexibility in the mechanical arrangement of things throughout a radar system – not just with signal processing. For example I could also choose to put the sensor up on a box on an antenna then do the digitization and send it across the fiber optic link at high speeds to an FPGA. "Pentek's latest FMC carrier board for radar applications has an optical backplane interface. The 3U VPX product – the Model 5973 – is the first one from of their new Flexor line of FMC (FPGA Mezzanine Card) carriers and FMC modules.

Some industry experts see general-purpose processors taking over more of the DSP functions of FPGAs, leaving them to focus on the RF side, while reducing the costs and time associated with programming FPGAs.

"Within signal-processing applications such as radar, there is a trend to do more of the DSP functions handled by FPGAs on a GPP," says Glenn Johnson, at Kontron in Poway, Calif. "This can make the design process more efficient and less costly as programming FPGAs in VHDL is still difficult and expensive. FPGAs in recent years have been able to do things that processors were never able to do. They started out on the RF end and progressed backwards to where they obsoleted DSP chips and ended up doing general processing. Now, thanks to advances with chips like the Intel Haswell device, the GPP is taking that burden off of the FPGAs, enabling them to focus on the RF receive and transmit chains." Kontron's Haswell offerings include COM Express, Mini-ITX, 6U CompactPCI, and SYMKLOUD products.

Haswell and military signal processing

While designed more with the gaming industry in mind, Intel's 4th generation Core i7 iteration, originally codenamed Haswell, has military signal-processing designers as excited as a teenager with a new Xbox on his birthday. Often working in tandem with FPGAs on a board, the device is enabling leaps in computing performance.

"Intel dramatically improved the AVX 2.0 math instructions, which on an SAR algorithm can improve performance by as much as 50 percent," says Eran Strod, Systems Architect at Curtiss-Wright Controls Defense Solutions. "Also, following the tenets of Moore's Law, the device takes up less die space and has these tiny tiny graphics execution units that provide hundreds of MFLOPS. For example our 6U CHAMP-AV9 boards with Haswell will be running at 1.2 teraflops – that's five times faster than current devices."

"Haswell will enable radar/EW system performance enhancements with functions such as pulse compression, beamforming, Doppler processing, etc.," Mercury's Couture says. "AVX 2 enables it to do the linear math and DSP necessary for radar signal processing at very high speeds. Another advantage with Haswell is on the power-management side, improving performance per SWaP at the individual core level. Essentially it will slow down certain cores that are running less taxing tasks while speeding up others performing intensive tasks. The primes like Haswell because it can attack more channels with wider bandwidth providing for more coverage in the electromagnetic spectrum at any given time."

"What's disruptive about this product is the larger bandwidth and spectrum digitization, which improves not only the radar system's ability to identify and track targets but also helps it avoid detection," says Bill Pilaud, Continuum HPEC Manager at Curtiss-Wright Controls Defense Solutions. "You protect the warfighter by sending information in one band and then switching to another instantaneously, moving the signal around faster than anyone can track it."

Saving costs through software development

Budget cuts and sequestration have the U.S. military looking everywhere to save pennies without compromising performance. In signal-processing systems they are achieving this though modular, open architectures that can leverage existing software code across multiple platforms.

"There is a lot of pressure to cut costs and to do that the integrators are looking deeper into the supply chain for help with integration," Curtiss-Wright's Strod explains. "They are looking for more re-use of software code from platform to platform to save on what can be extremely expensive development costs. They want to be able to take one platform-development effort and leverage it into multiple platforms."

"Radar customers don't just want open architectures, but to a large degree they want modularity in the system as a whole," Thompson says. "They are looking at the entire system and breaking it up into pieces and want to have different interfaces for hardware and software to make it far easier to change individual pieces of the chain without affecting pieces to the left and right of it.

"That is starting to have an impact on what they want from embedded computing companies like GE Intelligent Platforms," he continues. "In the past we would provide the hardware implementation of a radar processor, but now we are seeing a push to provide software solutions – not the radar application, but providing a level of middleware that is maybe more tilted toward the application than with previous applications. Before Haswell, GE started combining

CPUs and GPUs on a single board with three-quarters of a teraflop in a single slot and now we have a sister product in 3U and 6U SBCs with Haswell in a VPX architecture."

The cost of software development can also be quite high when upgrading to a VPX system from a legacy VME design. Sometimes users will shy away from it because of this, "so we are helping our customers port the software," Couture says. Mercury did this with their upgrade of the Patriot Missile Defense System radar. "To be specific, Mercury didn't compose or tamper with the customers' algorithms of application code, but we did migrate the DSP libraries and the fabric infrastructure 'plumbing' right underneath their application. That brought them from 1990s technology right into the 2010s."

Parallel compute languages

Open-standard software-development tools also are giving signal-processing system designers another way to reduce costs and development time. "When integrating systems with Haswell chips, FPGAs with ARM cores, etc., there are challenges in the upfront development process with time and expense," Couture says. However, tools such as CUDA and OpenCL enable designers to work across processing platforms, with hardware no longer a dominating cost in terms of product development. Algorithm and infrastructure development are where the most expense is incurred in signal-processing designs. The trend is for the signal-processing system vendor to help lessen that burden for the end user. With open systems such as OpenVPX, there is a greater focus on software development and managing the associated costs, which can be extreme. However, parallel compute languages such as CUDA and OpenCL enable designers to work across processing platforms to reduce these costs.

"CUDA is efficient with NVIDA GPUs and the Corefire tool from Annapolis works really well – but only with Annapolis products," Couture continues. "OpenCL, however, is the first thing I've seen that Texas Instruments, AMD, Xilinx, Altera, ARM, and Intel all support – and the list is growing." **MES**

SIGNAL PROCESSING TRENDS IN RADAR, SONAR, AND ELECTRONIC WARFARE

Using high-performance SRAMs to increase performance in DSP-intensive applications

By Suhail Zain

Military applications such as radar, Software Defined Radio (SDR), smart munitions and target-detection systems, Electronic Warfare (EW), aircraft imaging, and many more benefit from Digital Signal Processors (DSPs). DSPs accelerate performance using deterministic processing and have capabilities that include real-time signal processing, extremely high throughput, and reprogrammability. However, signal processing demands for radar, EW, and other programs continue to increase so DSP system users continue to search for innovation that will boost performance. That need is being answered by use of a combination of Quad Data Rate (QDR) Static Random Access Memory (SRAM) that – at a minimum – doubles the performance of more traditional Synchronous Dynamic Random Access Memory (SDRAM).

Petty Officer 3rd Class Andre Estrada, assigned to Electronic Attack Squadron 134, inspects the radar of an EA-6B Prowler aboard the flight deck of the aircraft carrier USS Carl Vinson (CVN 70). DoD photo by Petty Officer 2nd Class James R. Evans, U.S. Navy.

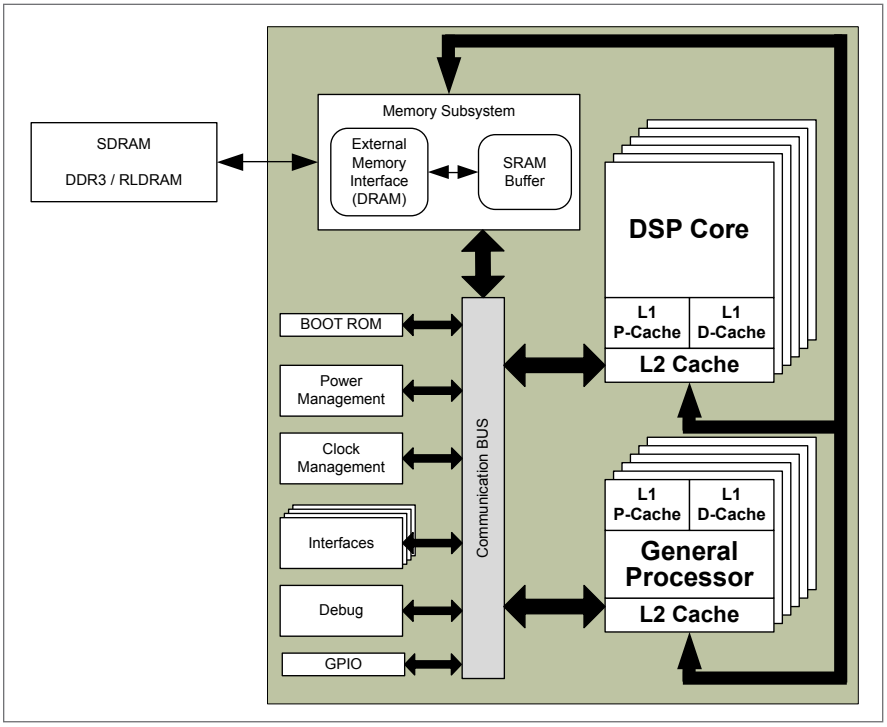


Figure 1 | TI's multicore DSP architecture.

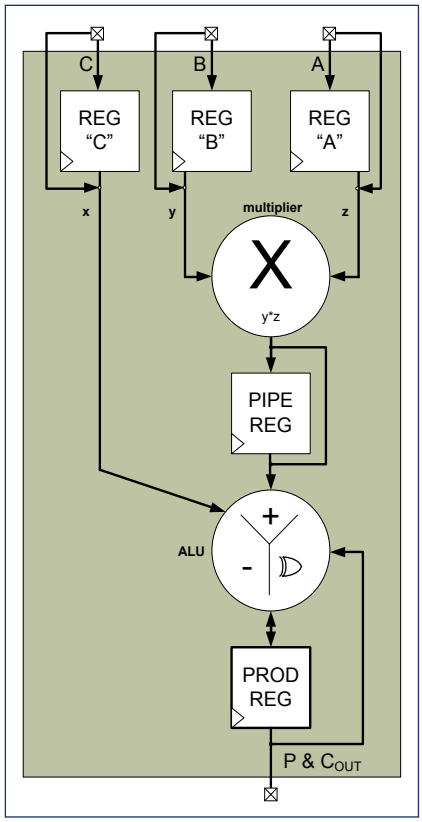


Figure 2 | Xilinx FPGA Virtex DSP architecture.

Digital signal processing

Digital signal processing encompasses techniques to manipulate signals after they have been converted into digital form as seen in radar processing. They are used for several functions in radar systems such as pulse compression, signal filtration, and pulse modulation. These components differ from general-purpose microprocessors in that they are designed for the types of fast mathematical calculations (multiplication and addition) most commonly used to design filters like FFT and Finite Impulse Response (FIR). Typically, FFT filters are used for domain conversion – time to frequency and vice versa – whereas FIR filters are used for signal separation and signal restoration.

There are two main hardware approaches for implementing DSPs: programmable DSP processors and FPGAs. In both approaches, the DSP architecture is optimized for DSP algorithms.

DSP processors

DSP processors like TI's multicore DSP processor (shown in Figure 1) have specialized hardware to compute multiplication operations in one cycle. The instruction set of modern DSP processors enables programmers to specify several parallel operations in a single instruction, typically including one or more data fetches from memory in parallel with the main arithmetic operation. Furthermore, to significantly improve the DSP work per clock cycle, DSP architectures now include additional multipliers and adders for parallel execution, thus encoding parallel operations in a single instruction.

FPGA-based DSPs

FPGAs like Xilinx's Virtex, shown in Figure 2, have dedicated DSP blocks to efficiently implement DSP algorithms. Each DSP block includes dedicated hardware-based functions such as multiply, multiply/accumulate, add, shift, compare, bit-wise logic functions, and pattern detect. Wider mathematical functions can be realized by cascading multiple DSP blocks together.

DSP memory requirements

Executing DSP functions every cycle requires the ability to fetch instructions and data from memory efficiently. This requirement means that high memory bandwidth is paramount to maintaining DSP performance. DSP processors, as well as FPGA DSP blocks, have developed internal cache memory architectures (L1/L2) to support multiple memory accesses per cycle. A Super Harvard Architecture is implemented where separate memory banks exist for instruction and data storage. With this arrangement, the processor can fetch both instructions and data operands in parallel every cycle. Moreover, memory accesses in DSP algorithms typically present a predictable pattern. For example, FIR filter coefficients are accessed sequentially and in a circular fashion. For deeper external storage, hardware-based External Memory Interfaces (EMIF) supporting various SDRAM memories (DDR2/3, RLDRAM) are typically employed. However, a new technique for external storage called Quad Data Rate (QDR) SRAM can improve DSP performance by a factor of two.

Improving DSP performance with QDR

QDR SRAM is a high-performance memory device optimized for high throughput. These memories have multiple independent data ports equipped with Double Data Rate (DDR) interfaces. Accesses to these data ports are concurrent and independent of each other. The address bus is common and

runs at either single or double data rate, depending upon the configuration. The highest density product available today is 144 Mbit and can be configured as x18 or x36.

The architectural features of QDR-IV SRAMs work favorably with the digital signal processing flow in applications where high throughput, low latency, and random accesses are required.

Traditional (SDRAM) vs. new (QDR-IV) approach

Figure 3 illustrates the general setup of the test environment. FPGA-based DSP functionality is used where the maximum data throughput from different memory types is compared. Table 1 compares the major performance parameters between QDR-IV SRAM and DDR3 SDRAM memory technologies.

The table shows that QDR-IV provides more than twice the DDR3 SDRAM bandwidth running at the same frequency. Moreover, the dual independent ports of the QDR-IV SRAM facilitate a DSP's real-time processing requirements on data where the output signal is produced at the same time as the input signal is being acquired. Using the QDR-IV, the bottleneck in transferring data to and from memory is alleviated.

SAR radar perspective

Synthetic Aperture Radar (SAR), which observes the Earth's surface in high resolution, needs corner-turn memory access where the range direction and the azimuth direction are transposed for reconstruction processing. This operation is done for efficient FFT and IFFT (DSP) execution between range and azimuth compress processing. The architectural benefits of QDR SRAMs can improve SAR radar's performance by allowing fast and uniform memory access times. Figure 4 shows the corner-turn problem with SAR image reconstruction.

Using a conventional SDRAM memory, writing (as shown) of the SAR picture data ends up in a discontinuous address space, leading to a reduction in processor performance (in this case, estimated at roughly five times). Because QDR-IV's independent ports for reading and writing enable concurrent operations and random memory access, the processing penalty is mitigated.

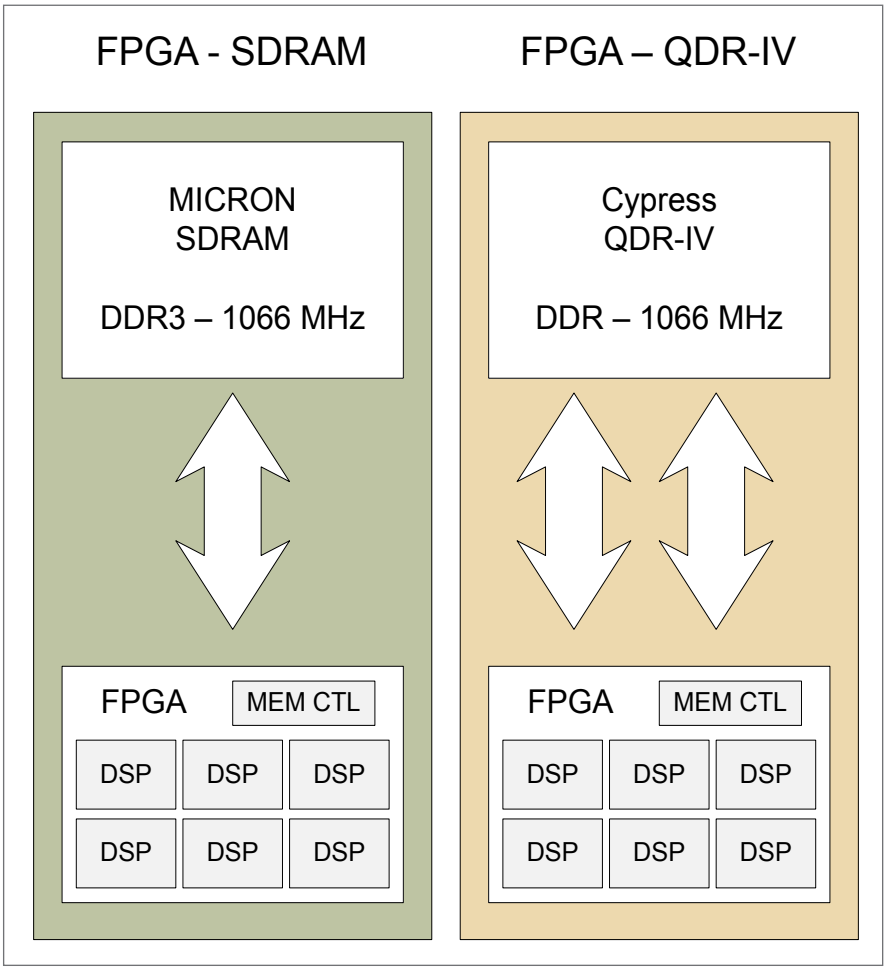


Figure 3 | Comparison of DDR3 SDRAM and QDR-IV SRAM test environments.

Feature	Cypress QDR-IV	MICRON DDR3
I/O Architecture	QDR Common I/O	DDR Common I/O
Addressing Scheme	DDR	SDR
Density	144 Mbit	8000 Mbit
Burst Length	2	4, 8
White Latency	5	9
Read Latency	8	14
Maximum Frequency	1066 MHz	1066 MHz
Peak Bandwidth	153.5 Gb/s	68.2 Gb/s

Table 1 | QDR-IV and DDR3 SDRAM comparison.

QDR SRAMs provide a beneficial performance alternative to conventional SDRAMs for off-chip data storage in DSP-based applications. Density limitation of QDR SRAMs can be mitigated by cascading multiple devices. This approach is ideal for applications where higher throughput with random access is required by enabling faster memory accesses for improved DSP performance. **MES**

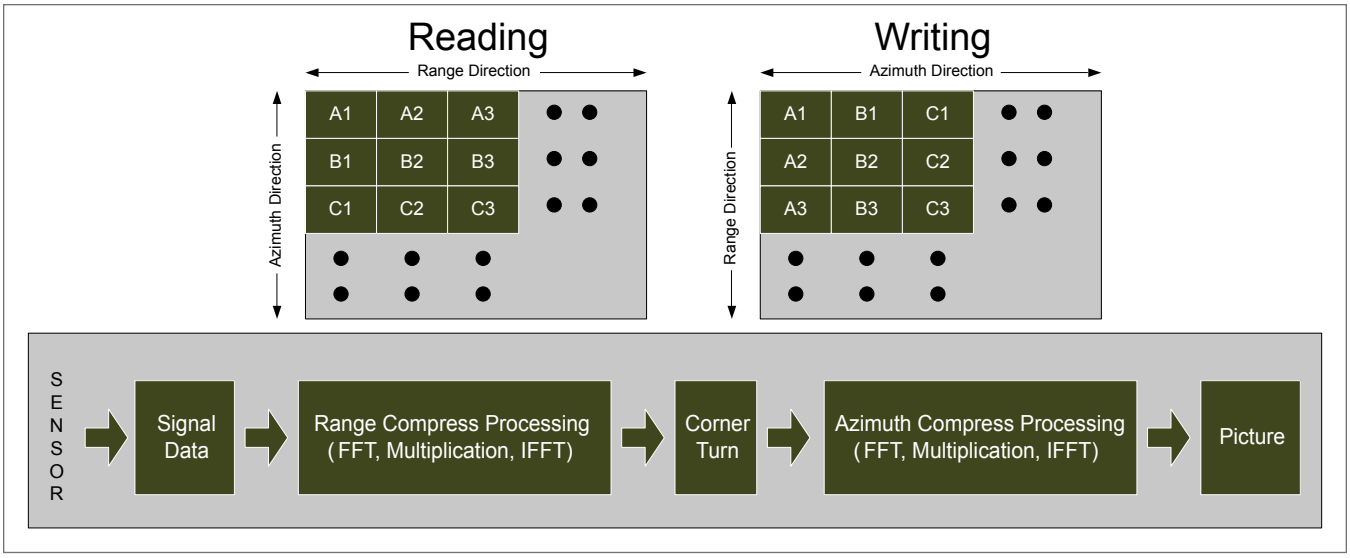
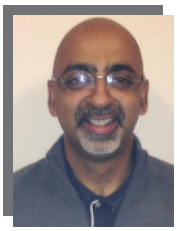


Figure 4 | Corner-turn with SAR image reconstruction.

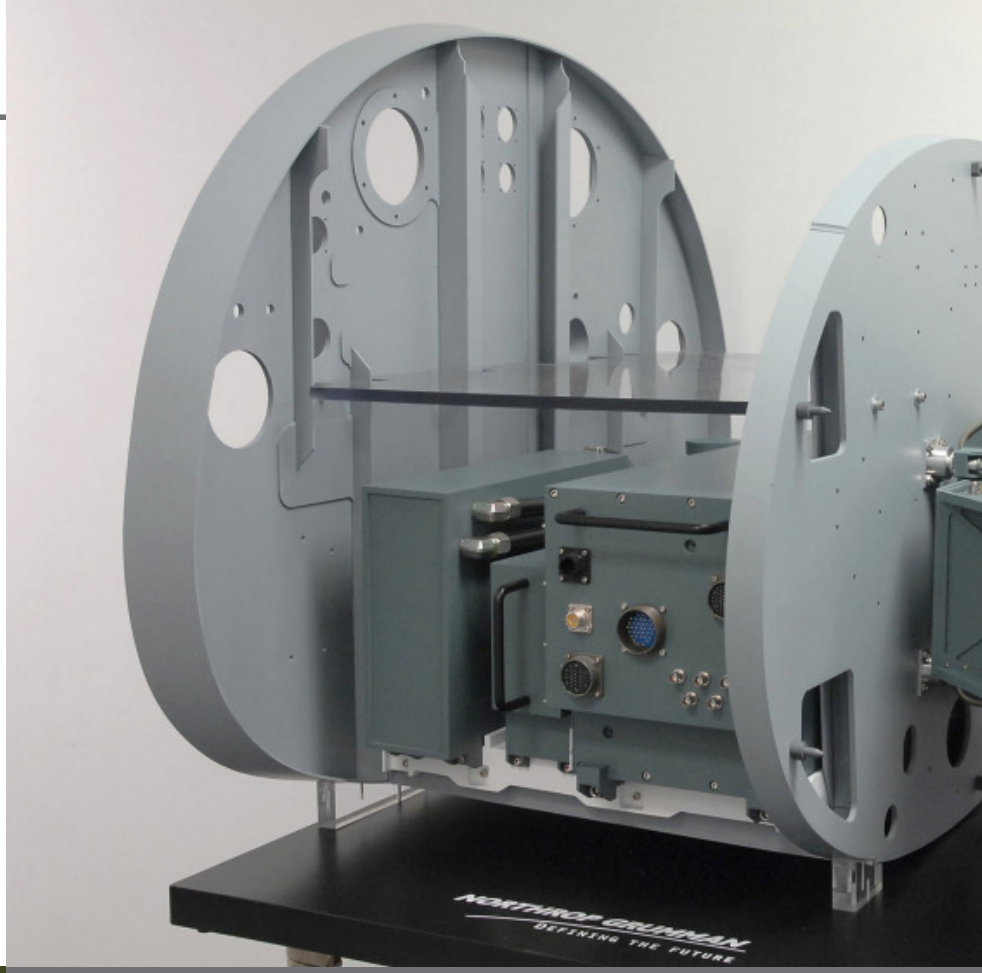


Suhail Zain *has been the director of new product development and strategic marketing for Aerospace & Defense at Cypress Semiconductor since 2010. He has more than 20 years experience defining, designing, and bringing to market state-of-the-art semiconductor products in reprogrammable technologies (FPGAs), high-speed memories (SRAMs), and trusted cryptographic solutions (TPMs). He earned both bachelor's and master's degrees in electrical engineering from the University of Southern California, with special emphasis on VLSI design. He holds more than 10 patents in design architecture.*

Cypress Semiconductor • 408-943-2600 • www.cypress.com

Common EW and radar systems for emerging military missions

By A. Lorne Graves



The Scalable Agile Beam Radar (SABR) is a full-performance Active Electronically Scanned Array (AESA) derived from proven AESA technology for F-16 aircraft. SABR is designed for retrofit to existing F-16 aircraft and can be scaled to fit other platforms and mission areas.

Due to shrinking Department of Defense (DoD) budgets and ever-decreasing platform size, the need to use common apertures and sensor chain elements for Electronic Warfare (EW) and radar systems is becoming a necessity. System developers must use common elements from Radio Frequency (RF) to processing to build such systems. The linchpin of these types of sensor-based systems is the I/O interface between the RF and processing elements. FPGAs have traditionally been used as this I/O interface, but now they are serving as an integral part of the processing subsystem on common EW radar systems.

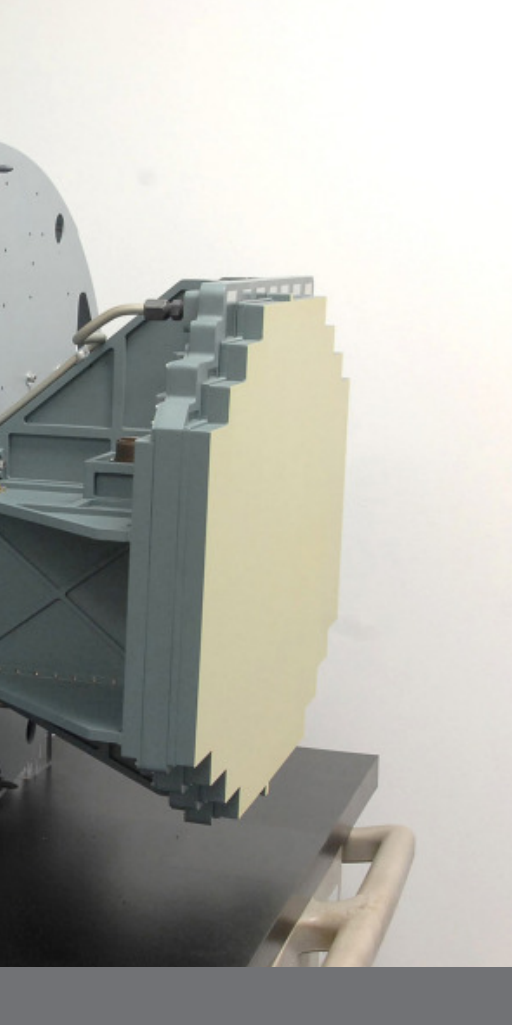
SWaP impacting military ConOps

As sequestration begins to affect multiple programs and budgets continue to shrink, the DoD must look for ways to maximize the financial value across various programs. Not only is cost a major factor on today's platforms, but the need to reduce payload Size, Weight, and Power (SWaP) on small Unmanned Aerial Vehicles (UAVs) is also a necessity. As UAV operations move into areas with contested airspace, not only will radar and Intelligence, Surveillance, and Reconnaissance (ISR) systems be needed, but electronic warfare systems will become an essential part of virtually every mission.

To optimize performance across these platforms, electronic systems providers must rely on a Modular Open Systems Architecture (MOSA) as well as on commercially available products. Commercially available products help reduce the cost of systems by reducing Non-Recurring Engineering (NRE) expense and can free up developers to focus on system integration and algorithm development. This focus can result in an electronic system delivered in less time with optimal results and a lower overall system cost. Typically, radar and EW system design have been two separate disciplines that used similar components to produce electronic systems for vastly different requirements. The common element used in both these types of systems is the Field Programmable Gate Array (FPGA)-based I/O interface. Today's FPGA, as it has matured with Digital Signal Processing (DSP) power exceeding typical General-Purpose Processors (GPPs) and with integrated Advanced RISC Machines (ARM)-based cores that provide low-power-control logic, is now considered a vital asset in most EW and radar systems.

Common radar and EW systems

To understand how FPGA processing plays a major role in fused radar and EW systems, it is important to first review a typical airborne radar system and then a typical EW system. Review of these two systems allows for identification of areas of overlap within the hardware components of each system. A typical airborne radar system has an antenna aperture with a high-power transmit and receive switch. Four receivers and one exciter provide the RF-to-Intermediate Frequency (IF) conversion in the system. The conversion from IF to digital data



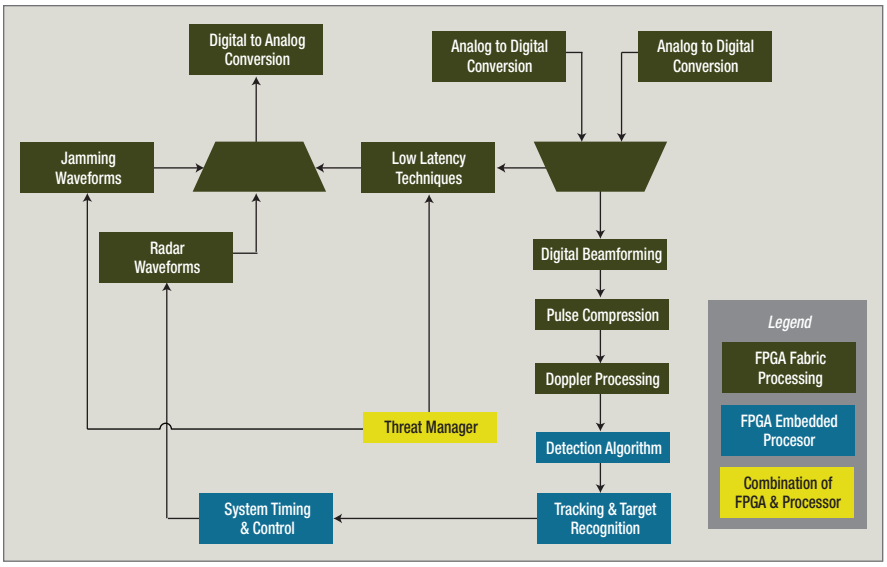


Figure 1 | Common EW and radar processing flow.

is performed on the FPGA processing element. Well-suited for beam-forming and pulse compression, the FPGA board will typically perform some elements of the radar processing; the FPGA processing element will provide the preprocessed data to the DSP elements, which then provide the detection, tracking, and target-recognition algorithms. The final element, a control processor, is responsible for network interfaces, control, status, and low-level control of the entire system.

EW systems tend to be broadband in nature, while radar systems are relatively narrowband. An EW system also contains an antenna aperture and has a wideband RF receiver and exciter, which provide RF-to-IF conversion. The conversion from analog to digital data is once again provided by the FPGA processing element, which also performs various operations to prevent enemy radar from tracking the platform. Countermeasures may include barrage jamming, spot jamming, and Digital Radio Frequency Memory (DRFM). FPGAs, due to their flexibility and adaptability, are able to easily handle the DRFM and other countermeasures. The DSP element in EW systems is typically responsible for determining what type of technique to use against enemy radar – therefore it is often referred to as a threat manager or scheduler. The DSP element and control processor are similar and may be one and the same in EW systems.

Typical radar and EW systems use common elements throughout. While the system bandwidths may vary greatly, the EW systems overlap those of the radar systems. For example, if a radar system is working within X-band (8-12 GHz), the typical EW system covers VHF through Ku band. Therefore, the antenna, RF receivers, and exciters for the EW system could be adapted for use in the radar systems. There are numerous tradeoffs (outside the scope of this article) that need to be made to develop common antenna and RF elements, however, such as the fact that the IF/analog conversion rates are very similar but the instantaneous bandwidths of the signals vary widely. Today's latest data-converter products offer sufficient resolution (dynamic range) and frequency coverage to be utilized in both systems. The I/O interface from the data conversion to the processing domain has already been dominated by the FPGA for years. The processing elements developed by commercial companies have become commonplace in both radar and EW systems. In fact, the use of open standards and operating systems like Linux has made COTS processing boards easily adaptable for both types of systems.

FPGA processing to unite radar and EW systems

FPGAs, once used as "glue logic" in most designs to "glue" interfaces together, have become processing workhorses in many of today's radar and EW systems. The maturation of FPGAs to include thousands of dedicated multipliers, highly optimized memory interfaces, and high-speed serial transceivers has turned them into one of an algorithm developer's favorite tools. With the integration of embedded low-power ARM processors into these devices, a new level of system fusion is becoming a reality.

The processing flow

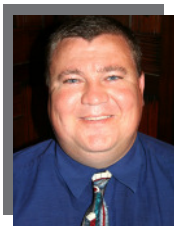
Typical radar systems use the FPGA for digital beam-forming and pulse compression. Detection and tracking algorithms are then performed in processing elements such as Intel- or Freescale-based GPP boards. With dual ARM cores available in FPGAs, there are multiple multi-GHz processing elements available to perform the detection and tracking algorithms. To enable the EW system, designers must take advantage of the same powerful building blocks within the latest generation of FPGAs. The EW processing flow – see Figure 1 – relies on the immense parallel-processing capabilities of the FPGAs. For example, in a DRFM countermeasure, the system designers may create multiple false

targets or create a Doppler shift on the radar return to "spoof" the enemy radar system. The EW system developer may also use the large amount of embedded memory in the FPGA to develop waveforms used in barrage or spot jamming. The final aspect of the EW system that may be performed in the FPGA is the threat manager. Again, the embedded processor is used as the control element in the system to develop the highly complex state logic needed to make the system a reality.

The ability to embed all of this functionality into FPGAs, while difficult, is now becoming a reality. COTS boards with multiple FPGAs can be partitioned to "fuse" the systems together. For example, latency-critical EW functions can be performed at the leading edge of the data conversion, followed by radar-processing elements. A high-level block diagram of a common FPGA-based processing system is shown in Figure 1. Mercury Systems offers products spanning from RF to processing; these products focus on delivering the full sensor chain to system developers.

EW and radar system fusion is becoming a necessity

With shrinking budgets and smaller platforms, EW and radar systems must begin to use common components to reduce Size, Weight, Power, and Cost (SWaP-C). U.S. DoD missions need to operate for longer durations and function in highly contested airspace. Leveraging COTS technology for FPGA processing elements and taking full advantage of the technological leaps in FPGA computing power, the fusion of EW and radar systems is rapidly becoming a necessity. As warfighters and the platforms they use are asked to do more with less, this fusion will give service members the capabilities to protect themselves and execute missions across the globe. **MES**

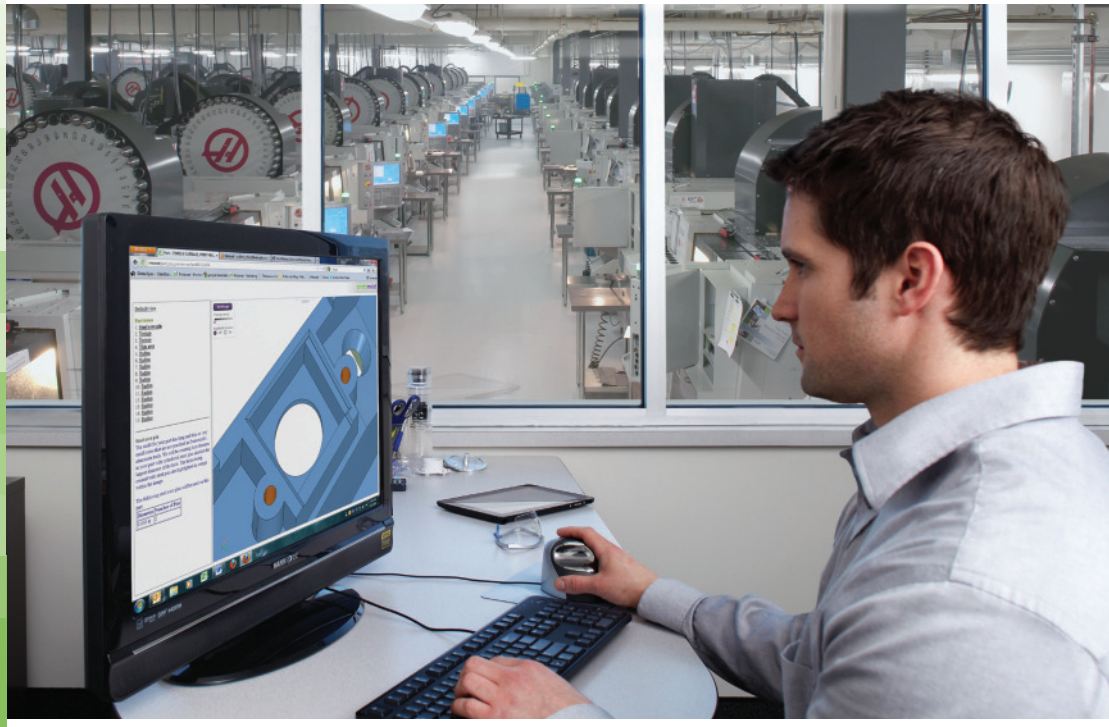


A. Lorne Graves is the lead architect for IF, Digital, and Integrated RF/IF products at Mercury Systems. With more than 20 years of experience designing mixed-signal circuitry and FPGAs as well as expertise in mixed-signal and RF technology, he has served as the business development lead on several key radar, SIGINT, and electronic warfare programs, working directly with various defense prime contractors. He was a key contributor of the architecture for the award-winning SCFE (VME and Critical Systems *magazine) product. Before joining Mercury in 2003, he was a senior engineer for a major networking company, and prior to that, he served as a Field Applications Engineer (FAE) for two electronic component manufacturers. Mr. Graves earned his bachelor's degree in electrical engineering from the University of Alabama, Huntsville. He can be reached at agraves@mrcy.com.*

Mercury Systems
866-627-6951
www.mrcy.com

Others say they're FAST...

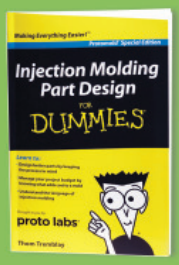
But do they have the SCALE to deliver?



Proto Labs' entire operation is optimized to deliver quick-turn CNC machined and injection molded parts in as fast as one business day. We manufacture parts every day for thousands of customers, many of whom come to us at the last minute with dozens of designs they need to test ASAP. Since 1999, we've produced tens of thousands of molds, and shipped tens of millions of parts to our customers all over the world.

Sure, it's our technology that allows us to make your parts faster than anyone else. We back it up with large-scale global manufacturing facilities with hundreds of CNC machines and injection molding presses on three separate continents.

Whether your project calls for a few machined parts or thousands of molded parts from 50 different designs—we have the scale to meet your needs. Every time!



Injection Molding Part Design for Dummies

Find out how to get better parts faster by understanding the basic principles of the injection molding process. Request your free book at **protolabs.com/parts.** Enter code MY14A.

Visa/Mastercard Accepted

Call 877.479.3680
or visit www.protolabs.com

ISO 9001:2008 Certified • ITAR Registered

proto labs®
Real Parts. Really Fast.™

Fusing video and radar tracks in multisensor military security

By Dr. David G. Johnson

Cambridge Pixel's radar scan conversion solutions are deployed on the British Royal Navy's Type 45 destroyers.

Effective fusion of multiple sensors such as radar video and cameras is the key to presenting a situational display in military security applications that successfully informs the operator and supports critical decision-making. However, while track display with track fusion offers the benefits of simplifying the display presentation based on an assessment of threat, this approach is only as effective as the rules used to process, filter, and select the information. Complementing the processed display with the ability to show primary sensor data allows for simplified presentation of complex information where there is confidence in the data interpretation, while still permitting the operator to observe raw sensor data for manual interpretation, verification, or simply reassurance.

A complex military security system uses multiple overlapping sensors to provide coverage of an area of interest. Sensors include radars and cameras, which may be co-located and combined in range to provide near, medium, and long-range detection, or which may be at different locations to enlarge the geographical coverage. A moving target that is acquired by one sensor may then be tracked, with continuity of identity, across multiple sensors, ensuring that the operator is presented with a consistent view of the target moving through the coverage of multiple sensors. The challenge with this approach is to present sensor and processed data in a way that supports an operator in the interpretation of the situation, with neither too much data so that there is a risk of confusion, nor too little data where critical information may be missing.

Presenting the operator with a high-level interpretation of the scene requires automatic identification of targets from sensor data and subsequent fusion of those tracks across overlapping sensors. Removing the raw sensor data and presenting processed, filtered, and prioritized reports will simplify the display and ensure that the operator sees only the relevant information. The key is getting the processing right so that there is neither too much rejection of real targets of interest (probability of detection is maximized) nor too little rejection of false targets (probability of false alarm is minimized).

Displaying multisensor data

Figure 1 shows the situation of two overlapping radars providing enhanced geographical coverage around a security installation. This is typical of a security installation around a high-value asset that observes short-range targets (for example, as far as 5 km) with one radar type and uses a different sensor for longer-range targets (for example, as far as 50 km). The display shows the presentation of the radar video (yellow for a short-range sensor, orange for the long-range sensor). Automatic processing has analyzed the radar video to identify targets of potential interest; these are shown as track symbols in white. The display can be simplified, as seen in Figure 2, by removing

the primary radar display, leaving tracks alone. In this example, tracks may be derived from either single primary radar or two fused primary radars.

The track extraction activity is an automatic software process that is configured to create tracks after consideration of several scans of radar video, where a target-like response has a consistent appearance. The number of scans considered does affect the speed of detection, but consideration for longer time will reduce false alarms. A balance must be achieved between the two, with different application requirements preferring shorter acquisitions or lower number of false alarms. The presentation in Figure 2 has removed the sensor data and presented only the targets that have passed the detection criteria.

If there is some uncertainty in the interpretation of the high-level fused display of Figure 2, the operator may enable the display of the primary sensor data, as shown in Figure 1. This enhances the display picture by presenting the radar video as graphical layers. By using semitransparent colors, the additional information enhances the display, preserving the presentation of the overlays. A priority assignment of each layer, together with transparency in the graphics rendering, ensures that the display of the enhanced sensor video does not obscure the processed track labels. The objective is to present the sensor information in a way that aids interpretation of the security picture, but does not mask the presentation of other information.

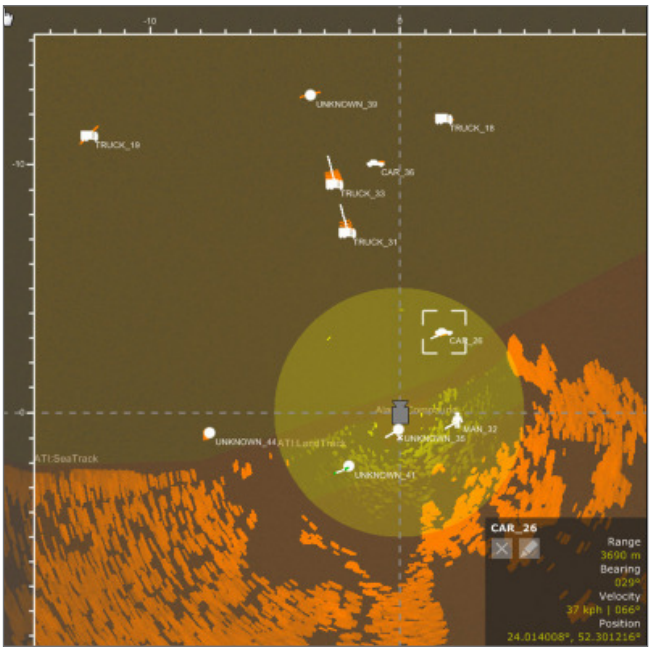


Figure 1 | Track data and radar video from two sensors.

Figure 2 | Display simplified to show track data only with radar video removed.

Fusing radar video

What isn't depicted by the screenshot of Figure 1 is the fact that the radar images are continuously updating with the sweep of the radar, typically at a rate of 30 times per second. This presents a moving radar sweep that matches the scanning of the radar, reassuring the operator of an active measurement process. The display processing that creates the multi-layered display is therefore combining scan-converted radar and graphics images at a rate of 30 times per second and compositing that data into a single image that is then copied to the display window. The processing involves a number of

stages that build layers of the display as an underlay map, add alpha-blended radars, and then draw the overlay. The choice of colors and degree of transparency in the alpha blending affects the appearance of the radar layers (from invisible to highly visible).

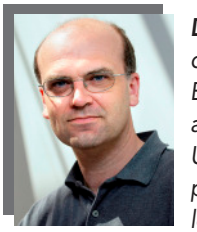
The combination of multiple images is comfortably handled by a modern graphics card in a Windows or Linux software application. The application shown in Figures 1 and 2 is a Windows application that runs on standard computer hardware. For larger screen sizes and multiple radars, a PCI Express graphics card accelerates the composition of the layers. Such a software solution is attractive to users because today's standardized single-board computers or desktop PCs can easily handle complex real-time graphics. The specialized hardware that historically underpinned this type of solution is no longer needed, and the software solution is flexible enough to give users the option to combine processed and real-time sensor information onto a single display.

As long as users take care to selectively enable the real-time data when requested or when uncertainty requires it, the result of this approach is a high-level display of fused information that is anticipated to be correct most of the time, but which has the backup of the sensor data to assist in challenging scenarios. **MES**

Case study – Kelvin Hughes' multisensor fusion

Surveillance company Kelvin Hughes, the developer of the SharpEye solid-state radar, teamed with Cambridge Pixel to source the core software components for its CxEye software processing and display solution for fusing video and radar tracks in multi-sensor security applications. Cambridge Pixel's SPx modular software – with its radar acquisition, scan conversion, multihypothesis target tracking, fusion, camera control, display, and C2 control functions – has allowed Kelvin Hughes to build the CxEye application with a modular, extensible architecture that offers a wide spectrum of surveillance solutions from single-sensor lone cameras all the way up to multiple nodes with separate command and control.

Using CxEye, multiple radars and cameras can be associated with a single node, permitting display of multiple radar videos, with tracks extracted and fused. Optical and thermal cameras under control of the node can also be automatically positioned based on radar track reports (slew-to-cue) and with track and image data uploaded to a remote command and control site. Importantly, in this solution, the operator has the ability to observe fused processed data as well as raw primary sensor data for verification.



David G. Johnson is technical director at Cambridge Pixel. He holds a B. Sc. degree in electronic engineering and a Ph.D. in sensor technology from the UK's University of Hull. He has worked in radar processing and display for 20 years and led teams developing software solutions for military radar tracking and radar scan conversion. Dr. Johnson can be reached at dave@cambridgepixel.com.

Cambridge Pixel
+44 (0) 1763 852749
www.cambridgepixel.com

Innovation **That Detects.**

Mercury Systems is a leader in developing software-defined subsystems that detect, intercept and defeat signals of interest — on land, at sea and in the air. These EW, SIGINT and C4I subsystem designs are born from our long standing expertise in analog, mixed signal and digital technologies. Because that's what it takes to combat next-generation electronic attacks.

Mercury also offers extensive core expertise in the design, development and manufacture of high-performance, spec-compliant RF microwave components. Our highly reliable product family consists of receiver components, noise sources, voltage controlled oscillators, linearized and non-linearized power amplifiers, and mixer and ferrite components.

Other Mercury Innovations

Big Data streaming analytics
Electronic countermeasures
High-density storage
High-performance computing
Mission security
Open EW architecture
Thermal management

MERCURY SYSTEMS™

INNOVATION THAT MATTERS™

Visit mrcy.com/SNFR to see how Mercury Systems' SIGINT and COMINT solutions deliver unrivaled capabilities.

Digital channelizer implemented on COTS FPGA board: A flexible solution for military signal processing

By Jeff Milrod

One of the major challenges of modern military Digital Signal Processing (DSP) is dealing with the ever-widening bandwidth of digitized signals. Until fairly recently, analog-to-digital converters (A/D converters) were limited to only hundreds of MHz, so anything beyond that had to be dealt with using traditional RF/analog methodologies. Now that A/D converters are available in the GHz range, much wider band processing is moving to the digital domain.

An EA-6B Prowler, which uses high-performance electronic warfare and radar systems, makes an arrested landing aboard the aircraft carrier USS George H.W. Bush (CVN 77) during flight operations. U.S. Navy photo by Petty Officer 1st Class Michael Tackitt.

For military and defense applications such as electronic warfare, electronic surveillance, radar, signals intelligence (SIGINT), and communications, the spectrum of interest can be as much as 20 GHz wide. Even the most advanced digitizers and signal processors can't directly capture or process that much bandwidth for general purposes. Using the same concepts that have been used for decades, the wideband RF must be broken up into narrower bandwidth "channels" via the analog receiver's front-end filters and mixers. Although this could be accomplished with a great multiplicity of channels – to the point where the resulting channel bandwidths are directly "digestible" by a digitizer and digital signal processor – this approach drives more complex analog front ends and more digitizers, resulting in increased size, weight, and power, along with additional performance challenges. The general desire is to get to digital as soon as possible, but digitizers have gotten so fast that it is often inconvenient or inefficient to digitally process such wideband channels. This reality has driven the need for a digital channelizer to further narrow the channel to a more optimally digestible width for downstream processing.

As an example, a 20-GHz spectrum might be broken down by the RF receiver into eight channels of 2.5 GHz each, which can then be digitized at 5 Gsamples/sec using readily available A/D converters. This is still a considerable bandwidth for downstream digital processing and feature extraction such as time of arrival and target identification. While digital processing could conceivably be implemented directly on such a wideband signal, there are several reasons to break it down into narrower bandwidth channels before processing, as is shown in Figure 1. Generally speaking, digital processing latency increases with bandwidth due to the need for larger filters and FFTs, so narrower bands reduce latencies. A narrower bandwidth will also capture less noise and irrelevant signals, so narrowband processing will result in higher signal-to-noise ratio results than wideband processing of the same signal of interest. In addition, processing power (GMACs) is proportional to bandwidth; in many applications where a large signal

bandwidth is under consideration, only a portion of that bandwidth need be analyzed at any given time. The channelizer allows the system to dynamically choose what portion(s) of spectrum to process, which reduces the necessary processing rate and power consumption compared to the full spectrum being processed all the time.

The system benefits of using a digital channelizer to further divide the incoming bandwidth before processing may now be clear, but how to implement one is not. Implementation requires creation of complex modulators operating on the incoming data stream, typically using filter banks created from DFTs, FFTs, and/or modulated cosine techniques, all of which involve detailed algorithmic and architectural tradeoffs. Although the underlying techniques are well understood, the implementation and optimization is quite complicated in practice.

FPGAs handle digitizing, channelizing

FPGAs are particularly well-suited for the task with their ability to directly interface to high-speed digitizers, in addition to their inherent processing parallelisms, hardened DSP blocks, and significant power advantages. At the same time, however, it is well understood that implementing complex algorithms, such as a channelizer, in an FPGA is challenging and difficult to both maintain and modify. Hardware design-flow challenges in this instance include writing behaviorally correct Hardware Description Language (HDL) algorithms; integrating components for I/O, control, and memory; minimizing resource utilization; optimizing latencies; and ultimately achieving timing closure. All of those challenges are revisited with each design iteration, modification, and specification change.

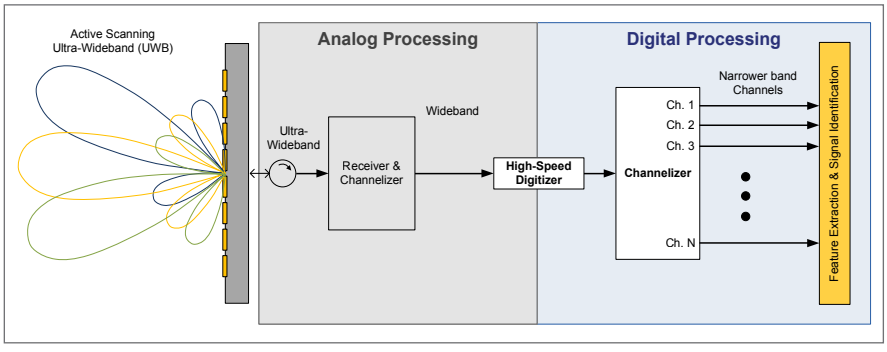


Figure 1 | System-level diagram of channelizer.

Well aware of these challenges, Altera has developed a complete channelizer IP block implementation for their DSP Builder tool. DSP Builder allows for high-performance push-button HDL generation of DSP algorithms directly from MathWorks' Simulink environment, providing a graphic block-level flow that delivers tremendous ease-of-use while automatically handling hardware design-flow problems. For example, the synthesis tool uses fused datapath techniques to reduce resources and latencies, automates timing closure, optimizes for device family and speed grade, and takes advantage of special hardware features such as DSP blocks. Algorithmic changes are performed in a Simulink-like environment in which users can take advantage of parameterization to experiment with relevant features, such as number of channels, to achieve the required system and hardware performance. In addition to this powerful and time-saving channelizer block, standard and advanced blocksets are also provided that can greatly simplify the implementation of processing the channelizer output for feature extraction and signal identification.

System-level FPGA project integration is also facilitated with Altera's Qsys system-integration tool, which saves significant time and effort during the FPGA design process by automatically generating interconnect logic to connect functions and subsystems, including DSP Builder algorithms. An integrated Qsys project implementing the channelizer is shown in Figure 2. Note that a complete 64-channel channelizer project, including the essential A/D converter interface, internal memory, and interconnects, takes only a small percentage of the FPGA's resources (depending, of course, on the specific implementation and FPGA size), leaving the vast majority of the FPGA's resources available for additional application processing such as feature extraction and signal identification.

With a channelizer core now available, along with an integrated FPGA example project, actual hardware is needed to deploy this integrated channelizer project in the real world, rather

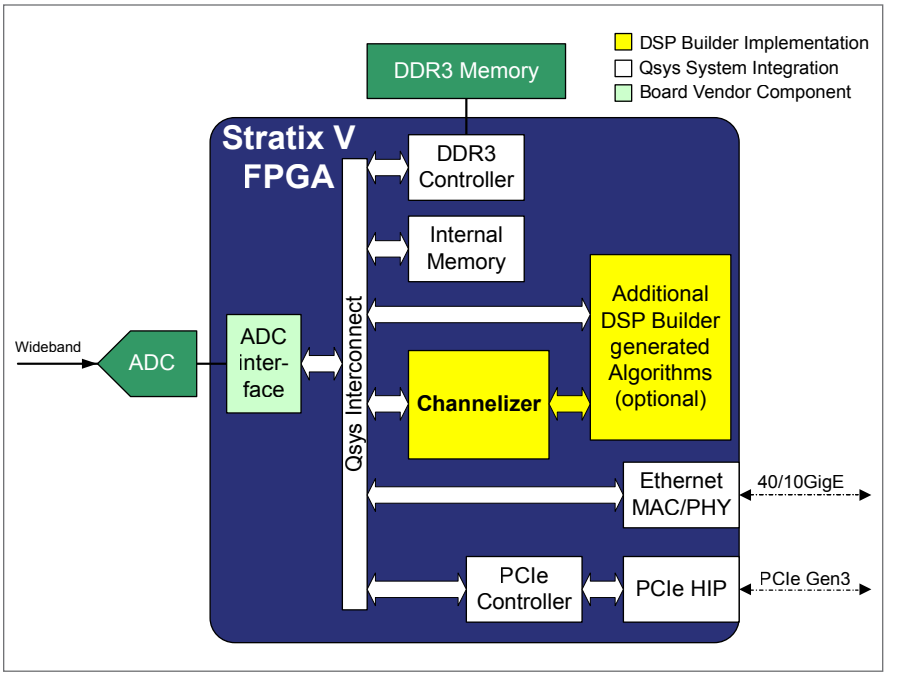


Figure 2 | FPGA implementation of a channelizer using DSP Builder and Qsys.

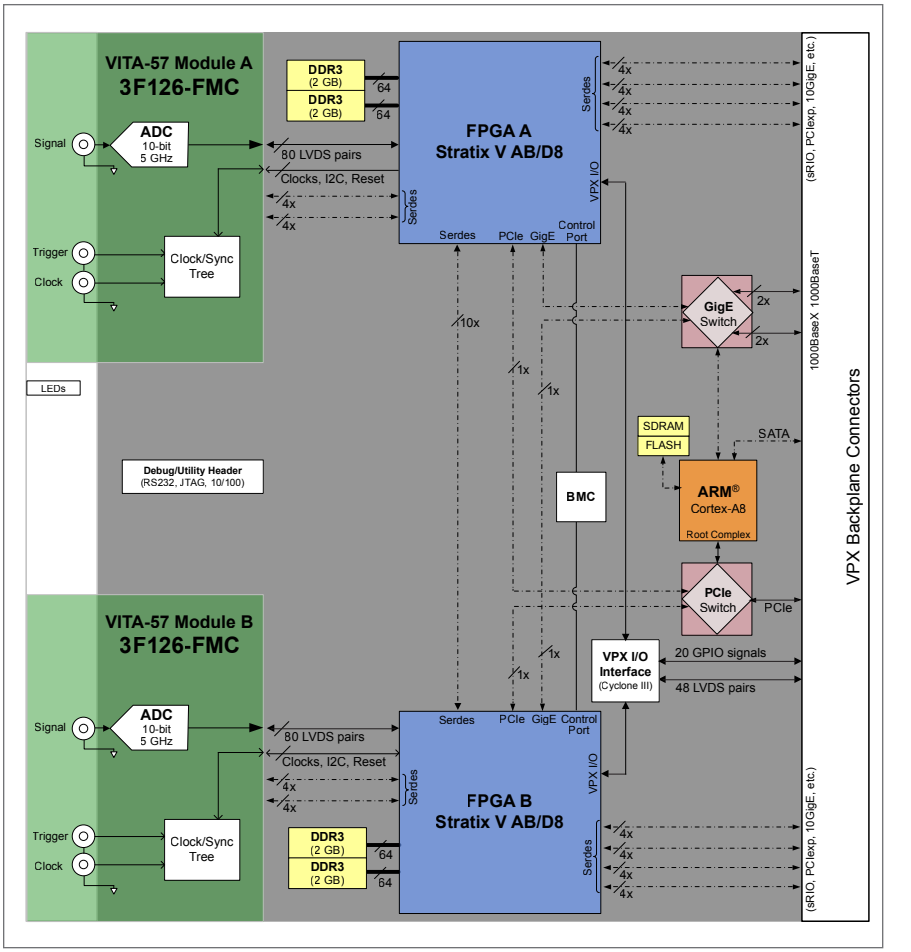


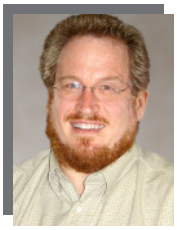
Figure 3 | S56X COTS dual-FPGA board fitted with 10-bit, 5-GHz A/D converters.

than just in a development and simulation environment. The COTS S56X 6U VPX board from BittWare provides two independent Statix V FPGAs, each with identical memory, communications, host interfaces, and VITA 57/FMC sites for modular I/O; this board can therefore support two separate instances of the channelizer project. The VITA 57/FMC sites can be populated with any number of A/D converters from Bittware or third parties to adapt the I/O for specific application requirements.

For the purposes of demonstrating the channelizer implementation and providing a reference platform, an FMC with a 10-bit A/D converter that runs at 5 Gsamples/sec was chosen and populated on both sites: the 3F126-FMC from BittWare as shown in Figure 3. The resulting board assembly can then be populated in a 6U VPX chassis, such as BittWare's VRDP-CH, with access to debug and communications via backplane, rear-breakout, and/or a separate breakout board. BittWare provides the A/D converter interface block that is integrated into the Qsys project; their standard software and support toolkit, BittWorks II Toolkit, provides the means to load, reset, and debug the FPGA and will monitor the board voltages, currents, and temperatures. The board's ARM processor, which runs Linux, is an on-board host/controller that can be used to implement command, control, and backend processing.

COTS solution

This reference platform provides a COTS solution for getting a wideband signal digitized and delivered to a well-supported FPGA which, when loaded with the example project, implements a complete wideband channelizer. Each FPGA parametrically "channelizes" 2.5 GHz of wideband input out of the box, resulting in each COTS board handling 5 GHz, with the bulk of the FPGA and ARM resources still available to the user. An ultra-wideband 20-GHz input can be easily accommodated by placing four of these S56X platforms in a 6U VPX chassis, providing a solution that is flexible, expandable, and scalable, all in a modest size, weight, and power envelope. **MES**

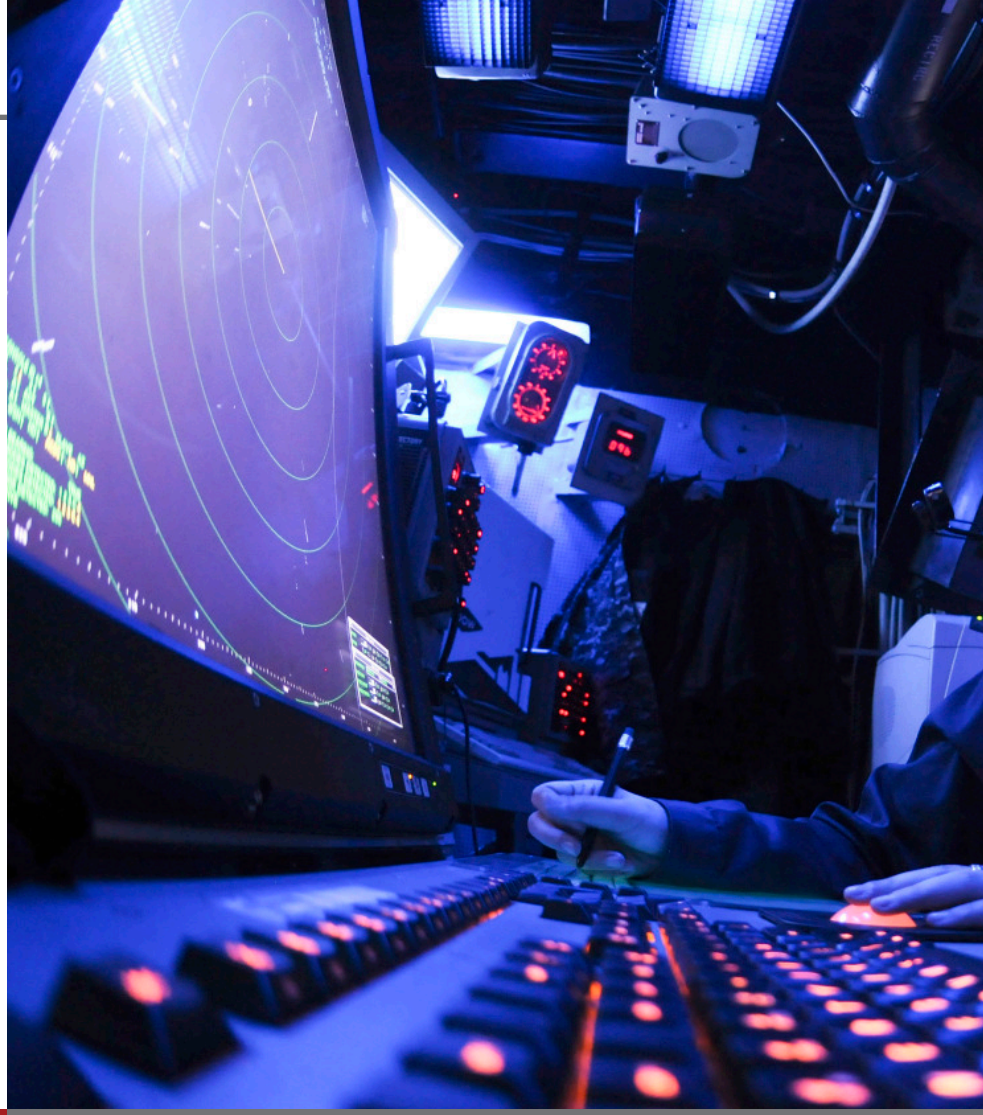


Jeff Milrod *– realizing the futility of pursuing a career in music (and reluctantly admitting his Dad was right) – went back to school and got a bachelor's degree in physics from the University of Maryland, and later an MSEE degree from Johns Hopkins University. After gaining extensive design experience at NASA and business experience at Booz, Allen & Hamilton, Jeff merged his technical expertise with his improvisational skills and started Ixthos in 1991, one of the first companies (along with BittWare) dedicated to COTS DSP. He ran Ixthos until it was acquired by DY4 Systems (now Curtiss-Wright Controls Defense Solutions) in 1997. Jeff left that company in 1998 and took the helm of BittWare, where he is President and CEO. Jeff can be reached at j_milrod@bittware.com.*

BittWare • 603-226-0404 • www.bittware.com

Designing a general-purpose FPGA DSP card for EW, radar applications using the latest generation of FPGAs

By Denis Smetana



U.S. Navy Airman Chelsea Pitchford monitors an air-approach radar console in the air traffic control center aboard the amphibious assault ship USS Essex (LHD 2). DoD photo by Petty Officer 2nd Class Greg Johnson, U.S. Navy.

Designing a general-purpose FPGA card that addresses the universe of Electronic Warfare (EW) and radar applications is a challenge. For any individual application, defining the requirements of the system and determining the optimal architecture for that particular solution is fairly straightforward. However, the problem is much more complex when trying to target a wide spectrum of use cases with a single FPGA module. The goal is to provide a flexible architecture that also enables the use of the latest FPGA features.

Sensor interface

The primary purpose of an FPGA card in a DSP system for EW and radar applications is to perform front-end sensor processing, which requires a high level of parallel processing as well as adequate and flexible I/O. To process and/or generate "real" data, the DSP system must convert analog and digital data using an Analog-to-Digital Converter (ADC) or a Digital-to-Analog Converter (DAC). Conversion can be done on the FPGA board, on a mezzanine card, or on a separate board. If conversion is done on the FPGA board, the ADC/DAC processing parameters – such as sampling rate, resolution, ENOB, and SFDR – are limited by its components and can't be changed easily. This approach, however, may simplify thermal management and often offers higher performance. Conversion on the FPGA board is preferred if the performance requirements can't be met using a mezzanine card; for example, if the connector from the mezzanine to the FPGA board is unable to handle the required bandwidth.

A more flexible option is to provide mezzanine sites on the FPGA card. VITA 57.1 FMCs (FPGA Mezzanine Cards) enhance an FPGA board with an open-standard, high-density, highly configurable interface for FPGA I/O. Popular with designers of FPGA boards for DSP and EW applications, the FMC approach delivers access to numerous off-the-shelf ADC, DAC, or mixed ADC/DAC mezzanine card options. The third option is to use a separate, dedicated board for FPGA I/O, sending converted data to the FPGA board via serial interfaces such as SFPDP or 10 GbE. Using this approach, the FPGA board requires a high number of SERDES (Serializer/Deserializer) connected to the backplane. Today's newest FPGAs feature numerous >10 Gbps SERDES to facilitate this capability.

EW applications require an extremely low latency path between the incoming

signal to the ADC and the outgoing signal to the DAC. To minimize latency, the incoming signal path should traverse through a single FPGA. This can be accomplished by using one of an increasing number of mixed ADC/DAC FMCs and mixed ADC/DAC monolithic boards available today. Alternatively, two mezzanine sites can be connected to a single FPGA. Because round-trip latency is not usually as critical for radar, ADC/DAC functionality can be separated. Channel synchronization, sampling rates, and resolution can vary for EW and radar applications, making a configurable ADC/DAC front end the optimal design solution.

FPGA processing relies on I/O, memory bandwidth

Each new generation of FPGAs increases speed, gates, and memory, and adds new capabilities. Figure 1 shows the approximate growth of logic cells delivered by recent generations of FPGAs.

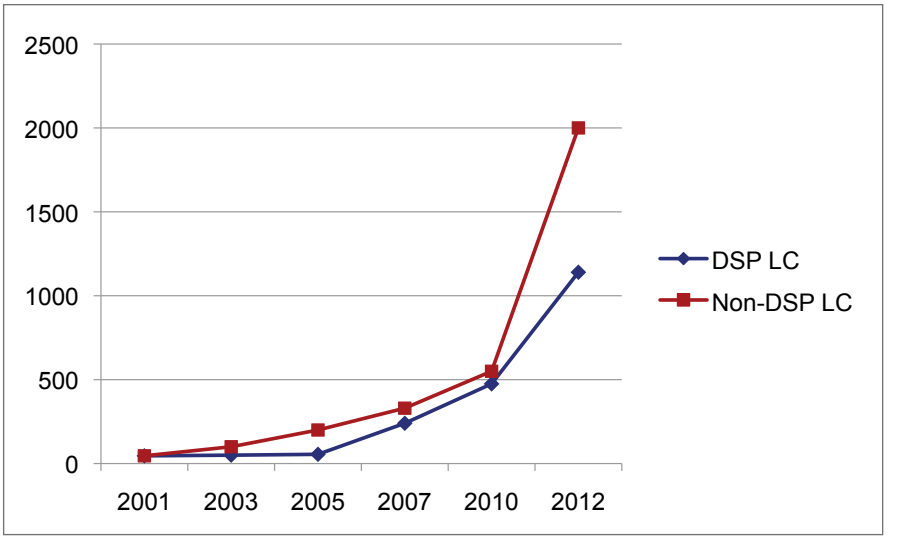


Figure 1 | Approximate FPGA logic cell growth for both DSP-centric and non-DSP-centric FPGAs.

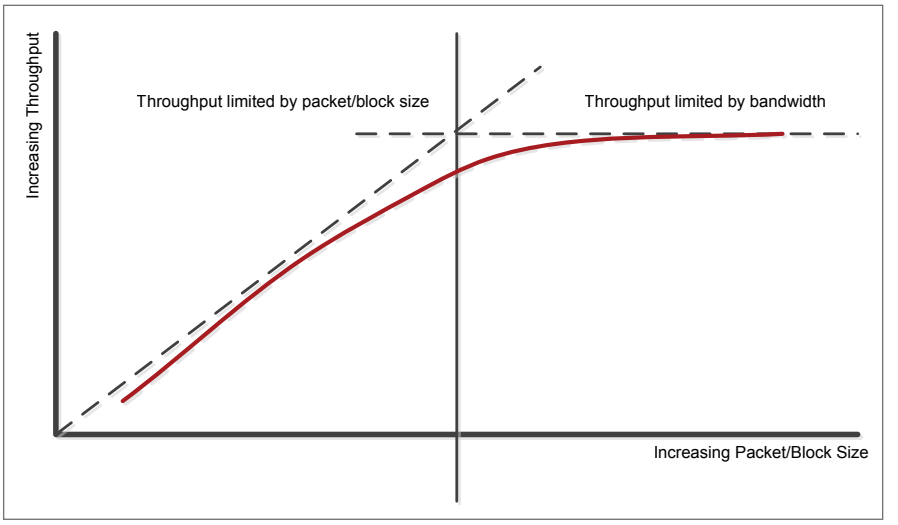


Figure 2 | Typical throughput graph relative to packet/block size.

An FPGA board designed to support both EW and radar applications requires a balance between I/O bandwidth, internal processing capability, external memory bandwidth and type, and interconnect options. If the I/O bandwidth or memory bandwidth is insufficient, then the increased FPGA processing capability cannot be fully utilized.

FPGAs and memory types

Generally, EW and radar FPGA applications require two types of memories: SDRAM for large bulk-data capture or delay chains, and SRAM for low latency or random access functions. SDRAM memory has high latency, while SRAM memory has a significantly lower capacity. The best approach for a general-function FPGA product is to use both types of memory, while also providing sufficient bandwidth for the I/O. In this capacity it is important to remember that if data is flowing through memory, the combination of writes and reads will effectively halve the available memory bandwidth. This slowdown is documented in Figure 2. Furthermore, optimal use of memory bandwidth depends on the block or packet size, which can be affected by DMA capability – something that is particularly true for high latency SDRAMs. Algorithm designers need to consider

actual memory bandwidth when architecting data flows.

Both EW and radar applications are heavily DSP-centric, which means that in addition to using general-purpose logic, they can benefit greatly by having access to dedicated, hard-routed DSP resources. The latest FPGAs are ideal for these applications. The largest DSP-centric FPGAs contain thousands of hardened DSP blocks, containing optimized multiply-accumulate functions, and can perform more than five trillion fixed-point multiply-accumulate operations per second.

High-speed interconnect to handle data

At some point in the EW or radar application, the data on the FPGA card will need to be interconnected to other FPGA cards or processor cards. An industry-standard, high-speed interconnect – such as SRIO, PCIe, or 10/40 GbE – needs to be used so that the processor can handle the data. The newest FPGAs include Gen3 PCIe cores, and sometimes 10/40 GbE cores as hard macros, which help free up more resources for DSP functionality. It is also important to have Direct Memory Access (DMA) capability to send large blocks of data, thereby minimizing packet overhead. In-band interrupt capability is also desirable to minimize processing overhead and maintain data coherency.

For interconnecting FPGAs, a low-overhead protocol such as Aurora is usually the best option, as the speed is not limited to a specific frequency and can be adjusted as needed. In some applications, the ability to decouple the transmit and receive SERDES with Aurora is beneficial, because the transmit and receive links can then be daisy-chained from one FPGA to another.

As backplane architecture speeds reach 10 GHz, many techniques need to be implemented to ensure good signal integrity. These techniques include the correct selection of low loss, the use of smooth-weave PCB material, sufficient signal isolation, back drilling of vias to manage stub length, and the minimization of trace impedance mismatches. See Curtiss-Wright's new white paper, "The Importance of Signal Integrity: Achieving Robust Gen3 >10 Gbaud Signaling in OpenVPX Systems" (http://www.cwcdefense.com/media-center/whitepapers/signal-integrity.html) to learn the key considerations for ensuring signal integrity with VPX systems. One useful new capability provided by the latest FPGAs is the ability to observe the SERDES signal internal to the device at the receiver. This ability is a necessity when running at 10 GHz, as the signals cannot be monitored externally and need to be viewed after equalization. With advanced equalization capabilities such as Decision Feedback Equalization (DFE) built into the SERDES, dynamic and automatic adjustments can be made to the signal without user control, which is important when running over wide temperature ranges. Figure 3 shows the eye as seen internal to a Xilinx Virtex-7 FPGA, after equalization, and can be viewed while the system is running.

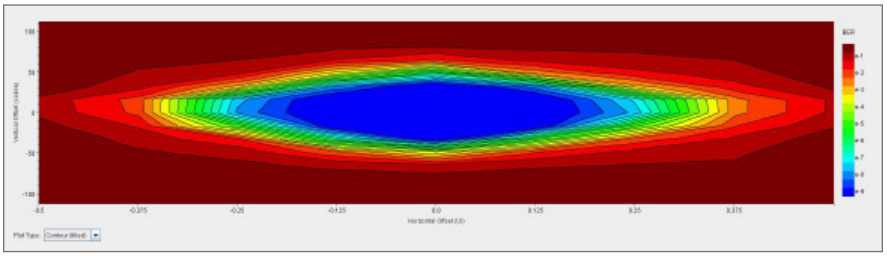


Figure 3 | Example of a 2D eye scan diagram. Image courtesy of Xilinx.

Reconfiguration easier with FPGAs

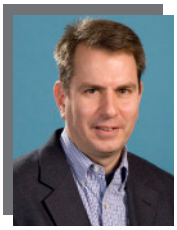
Reconfigurability is another key benefit of FPGAs. Their silicon can be easily reprogrammed to perform many different functions, or even many permutations of a similar function. Partial reconfiguration takes this concept a step further: Using partial reconfiguration, most of the FPGA design remains constant (and active), while only a portion is modified in real time. One new capability supported by the latest FPGAs is reconfiguration directly over PCIe, enabling the processor to adjust the design in real time. These characteristics of FPGAs provide the enhanced degree of adaptability that proves ideal for addressing ever-changing EW threats.

Thermal considerations

For both EW and radar applications, processing must be performed in harsh environments. This factor requires components that have wide operating temperature ranges and the use of cooling strategies that minimize the die temperature as much as possible even as power consumption grows. FPGAs, like other processors that use small-dimension silicon geometries, tend to have relatively high leakage currents. Leakage results in static power consumption that is very temperature-sensitive and can cause large power increases at high temperature. Sufficient cooling of today's high-powered FPGA boards demands advanced modeling, design, and materials, so it is important to understand the thermal profile used to design and test the card to ensure that the ultimate application fits within those parameters. With FPGAs, power consumption can vary drastically with respect to utilization, clock speeds, and the "switching factor" of the design. FPGA designers and vendors, when possible, should use tools like clock gating to help optimize power consumption. Built-in temperature sensors on the FPGA die, along with other current and temperature sensors on the board, can help provide valuable feedback during development and operation.

Considerations for FPGA hardware

When looking for the optimal FPGA hardware for EW and radar applications it is important to consider board and system architecture, I/O bandwidth, sensor-interface options, memory bandwidth, FPGA processing capability, and ruggedization capability to ensure that the hardware can support the target application. **MES**



Denis Smetana *has worked for 10 years on FPGA products for defense applications at Curtiss-Wright, starting as an FPGA designer, rising to product development manager, before moving into his current position as the product marketing manager for FPGA products. He has more than 25 years of experience with ASIC, FPGA, and hardware development, starting as an engineer developing ASICs and FPGAs for IBM's Federal Systems Division. He then developed and managed ASIC development for telecom applications utilizing real-time traffic for Integrated Telecom Technology and PMC-Sierra before joining the Curtiss-Wright team. Denis has a BSEE from Virginia Tech. He can be reached at denis.smetana@curtisswright.com.*

Curtiss-Wright
973-541-3700
www.curtisswright.com

Radar Product Spotlights

Protocol Converters

- Already Qualified! (MIL-STD-461, MIL-STD-704, MIL-STD-810, MIL-E-5400T)
- ARINC 429, MIL-STD-1553, RS-232/422, SYNCHRO
- Multi-Protocol
- Firmware allows the unit to operate completely transparent – acting as bridge between systems
- Operates from 28vDC
- Custom designs with little or no NRE with minimum quantity order

KIMDU CORPORATION

Kimdu Corporation
1-800-677-6174
www.kimducorp.com
sales@kimducorp.com

Wind River

- Safety-critical market leader – trusted on over 300 programs
- Open architecture support including ARINC 653 and FACE™
- DO-178C Level A compliant
- Highly flexible and configurable – single-core to multi-core, single-OS to multi-OS, mixed levels of safety & security
- Decades of experience powering space and terrestrial vehicles

WIND RIVER

Wind River
800-545-WIND (9463)
www.windriver.com

XPedite2470 – Virtex 7 FPGA-based 3U OpenVPX Module

- Eleven high-speed GTX lanes to VPX P1 connector
- VITA 57 FMC site for high speed DAC or ADC
- VITA 49 Radio Transport (VRT) support
- Freescale QorIQ P1010 processor with PowerPC e500 core
- Firmware Development Kit (FDK) and Software Development Kit (SDK)
- Supports 330T, 415T, 485T, or 690T Xilinx Virtex-7 FPGAs

X-ES Extreme Engineering Solutions

Extreme Engineering Solutions
608-833-1155
www.xes-inc.com

XPand6208 – High-Performance Small Form Factor (SFF) System

- 4th Gen Intel® Core™ i7 Processor with 10 Gigabit Ethernet
- Cisco® IOS™ Router and 10 Gigabit Ethernet Switch
- VICTORY infrastructure Switch and Router support
- Optional Removable Memory Bay for ruggedized 2.5 in. SATA SSD memory module
- Compact and lightweight Commercial-Off-The-Shelf (COTS) rugged system
- Utilizes two 3U OpenVPX modules and integrated MIL-STD 28 VDC power supply

X-ES Extreme Engineering Solutions

Extreme Engineering Solutions
608-833-1155
www.xes-inc.com

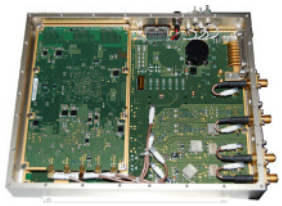
Thermacore delivers thermal performance advantages in the world's hottest spots

- Succeed with Thermacore thermal management technologies, delivering mission-critical solutions for advanced military systems since 1970.
- For military and aerospace applications on land, sea or air.
- Create innovative, reliable thermal solutions through our military-system engineering partnerships.
- Blend novel concepts and new materials with proven technologies.
- Learn more about improving thermal performance at Thermacore Design Center: www.thermacore.com/design

THERMACORE Thermal Management Solutions

Thermacore
717-569-6551
info@thermacore.com

Rakon's Digital Pulse Compression Sub-Systems (DPCSS)



- Digital technology for radar maintenance and life extension.
- Military and civil SAW based pulse compression radars.
- Low cost off-the-shelf expander and compressor unit.
- Customized unit, form, fit and function compatible with existing units.
- Improves overall system performance. High instantaneous dynamic range.
- High flexibility (programmable parameters), reproducibility and stability.

rakon synchronising connectivity

Rakon Limited
+33 4 97 97 97 32
www.rakon.com
sales@rakon.com

Radar Product Spotlights

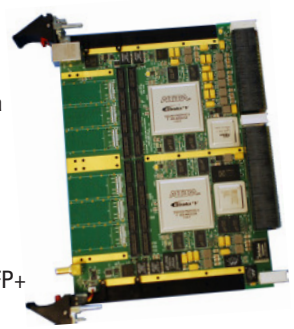
COTS WILD OpenVPX EcoSystem

- High Performance Signal & Data Processing in Scalable COTS FPGA Computing Fabric
- WILDSTAR FPGA Processing Boards – 1 to 3 Altera Stratix V
- WILDSTAR FPGA Processing Boards – 1 to 3 Xilinx Virtex 6 or 7
- 4, 6 or 12 Slot Custom Chassis – Up to 14G
- OpenVPX Storage – Up to 8 TBytes Per Slot
- OpenVPX Switch – 1 to 40 Gbit Ethernet, SDR to FDR Infiniband

Annapolis Micro Systems

Annapolis Micro Systems
410-841-2514
www.annapmicro.com
wfinfo@annapmicro.com

WILDSTAR FPGA COTS Processing Boards



- High Performance Signal & Data Processing in Scalable COTS FPGA Computing Fabric
- WILDSTAR FPGA Processing Boards – 1 to 3 Altera Stratix V or 1 to 3 Xilinx Virtex 6 or 7
- Up to 6 Optional Front Panel QSFP+
- Up to 24 10 GbpsE, 6 40 GbpsE or 6 14 Gbps FDR Infiniband
- Reduce Risk, Save Time, Save Money, Quick & Easy App Development, Standardize, Control

Annapolis Micro Systems

Annapolis Micro Systems
410-841-2514
www.annapmicro.com
wfinfo@annapmicro.com

COTS WILD Data Storage Solution

- Up to 8 TB Storage per Each 6U OpenVPX Slot
- Up to 16 SSDs per WILD Storage Board
- Up to 4 GB/s Write and up to 8 GB/s Read Bandwidth
- Up to 40 GbE or QDr Infiniband on each of 4 Fat Pipes for OpenVPX P1
- Hot Swappable Canister with up to 16 Pluggable 1.8" SSD SATA 3.X Drives
- System Management via IPMI, API for Command and Control

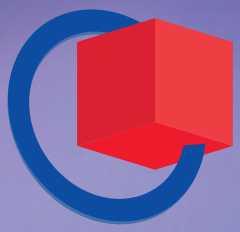
Annapolis Micro Systems

Annapolis Micro Systems
410-841-2514
www.annapmicro.com
wfinfo@annapmicro.com

Register now and secure your ticket!
embedded-world.de

Nürnberg, Germany

February 25 – 27, 2014



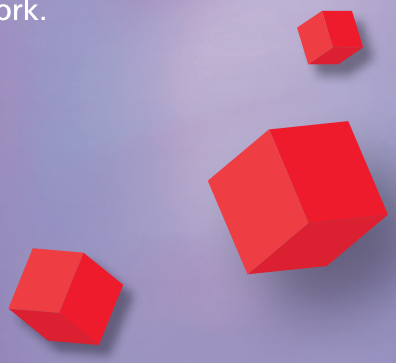
embedded world 2014

Exhibition&Conference

... it´s a smarter world

Summit for Innovations

The world's largest event for Embedded-Technologies is inviting you. The international Embedded-Community trends of tomorrow will be set right here! A must attend event, to establish contacts and expand your network.



Media Partners

elektroniknet.de
computer-automation.de
energie-und-technik.de
karriere-ing.de
Markt&Technik
Elektronik
Elektronik automotive
ENERGIE & TECHNIK
COMPUTER & AUTOMATION
MEDIZIN elektronik
DESIGN & ELEKTRONIK KNOW-HOW FÜR ENTWICKLER

Organizers

Trade Show
NürnbergMesse GmbH
Tel +49 (0) 9 11.86 06-49 12
visitorservice@nuernbergmesse.de

Conference
WEKA FACHMEDIEN GmbH
Tel +49 (0) 89.2 55 56-13 49
info@embedded-world.eu

NÜRNBERG MESSE

GE
Intelligent Platforms

High-performance RADAR with out-of-box readiness.

In today's rapid prototyping environment, RADAR system developers cannot afford to let performance and scheduling risks impact their projects. GE's rich subsystem development heritage coupled with our proven COTS components and state-of-the-art AXIS integrated software development tools virtually eliminate many avenues of risk. Our RADAR subsystems are shipped with high manufacturing and technology readiness levels that speed system development and reduce program costs.

Let our COTS-based computing and signal processing products help you boost the readiness of your next RADAR project.

defense.ge-ip.com

imagination at work

Got Tough Software Radio Design Challenges?

Unleash The New Virtex-7 Onyx Boards!

Pentek's Onyx® Virtex-7 FPGA boards deliver unprecedented levels of performance in wideband communications, SIGINT, radar and beamforming. These high-speed, multichannel modules include:

- A/D sampling rates from 10 MHz to 3.6 GHz
- D/A sampling rates up to 1.25 GHz
- Multi-bandwidth DUCs & DDCs
- Gen3 PCIe with peak speeds to 8 GB/sec
- 4 GB SDRAM for capture & delay
- Intelligent chaining DMA engines
- Multichannel, multiboard synchronization
- ReadyFlow® Board Support Libraries
- GateFlow® FPGA Design Kit & Installed IP
- GateXpress® FPGA - PCIe configuration manager
- OpenVPX, AMC, XMC, PCIe, cPCI, rugged, conduction cooled
- Pre-configured development system for PCIe
- Complete documentation & lifetime support

With more than twice the resources of previous Virtex generations plus advanced power reduction techniques, the Virtex-7 family delivers the industry's most advanced FPGA technology.

Call 201-818-5900 or go to www.pentek.com/go/mesonyx for your FREE online *Putting FPGAs to Work in Software Radio Handbook* and Onyx product catalog.

NOW AVAILABLE!
RF Slot Downconverters

Onyx

PENTEK
Setting the Standard for Digital Signal Processing

Pentek, Inc., One Park Way, Upper Saddle River, NJ 07458 • Phone: 201.818.5900 • Fax: 201.818.5904 • e-mail:info@pentek.com • www.pentek.com